

Article

Analysis and Designing of New Broadband Power Divider Using Stepped Impedance for WLAN and 5G Applications

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Abstract— The development of radio frequency circuits is currently guided mainly through two objectives, which are size reduction and performance improvement of devices. Within a reception or transmission channel, the division and/or combination of power are the most delicate stages due to their large dimensions and high insertion losses, particularly in the case of dividers/combiners based on planar technologies. In this context, this study proposes an analysis and design of a new broadband power divider and combiner using stepped impedance. The power divider/combiner developed is designed to cover a broad frequency spectrum ranging from 1 GHz to 4 GHz, including wireless applications such as Global Mobile Communications Systems (GSM), Industrial, Scientific and Medical (ISM), and Sub-6 GHz 5th Generation (5G) applications. The proposed circuit was analyzed using the stepped transmission line impedance method and designed by Advanced Design System (ADS) on an Epoxy-FR4 substrate with a dielectric constant of 4.4 and a thickness of 1.58 mm. The achieved results showed excellent characteristics in terms of transmission across the input and output terminals, mismatches at all three terminals, and isolation among output terminals. A prototype was built and the measured results showed good agreement with those obtained by simulation.

Index Terms— Broadband Power Divider, Fifth Generation (5G), Planar Technologies, Stepped Impedance.

I. INTRODUCTION

Rapid advances in modern mobile and wireless telecommunication systems have led to more and more dual-band or broadband RF and microwave circuits being developed in place of conventional structures to reduce system complexity, share resources, and reduce manufacturing costs and RF circuit losses as much as possible. Several broadband RF circuits have been designed to date, such as broadband filters [1]-[3], couplers [4]-[6], power limiters [7], mixers [8]-[10] as well as antennas [11]-[14]. Power dividers/combiners are also among the most popular RF circuits used in many microwave applications requiring wide bandwidth. Particularly, the broadband Wilkinson power divider/combiner has attracted increasing interest recently, as it has been useful in various microwave circuits, such as

amplifier chains, mixers, and separation of the receiver and transmitter chains when using a single antenna. Although the standard Wilkinson divider has a simple structure, it offers high performance, but its bandwidth is limited due to the isolation constraints affecting the output ports as well as its large size, which limits the use of this divider in many applications.

Several alternatives have been developed to obtain broadband power dividers, mainly for planar technologies, based on different design strategies. One of these is to find the port matching and isolation conditions directly by establishing certain design equations. In [15], the authors present the design of a symmetrical power divider consisting of nine transmission lines with the same electrical length and two isolation resistors separated by two transmission line sections. In [16], the authors proposed a Wilkinson power divider consisting of six transmission line sections and three isolation resistors using a dual-band topology to extend its bandwidth. In [17], the authors proposed a WPDC having a wide tunable bandwidth composed of nine transmission line sections along two isolation resistors while improving its bandwidth by adding a pair of capacitors. Furthermore, other approaches have been proposed to fulfill additional requirements such as compact size and dual-band [18]-[20]. Despite the numerous advantages of these techniques, they nevertheless suffer from the large size and use of lumped elements, which affect their performance in the microwave frequency band.

In this paper, a miniature planar Wilkinson divider/combiner based on wideband stepped impedance, which operates on the bands dedicated to multiple applications such as GPS around 1.5 GHz, DCS around 1.8 GHz, WCDMA around 2.1 GHz, WIFI, Bluetooth and the Sub-6 GHz band of the 5G technology is designed and implemented. The equivalent structure-specific dimensions were discussed according to the transmission line theory in the first part. Then, the design of the proposed structure has been examined, optimized, and determined. Finally, the results were discussed and a prototype was fabricated with a comparison provided of the proposed structure and the related recently published literature.

II. ANALYSIS AND DESIGN THEORY

The basic element of the power combiner used for the design of the power divider/combiner proposed in this investigation is the traditional Wilkinson power divider, comprising an input port connected through a quarter-wave transformer of characteristic impedance $Z_0\sqrt{2}$ to the output ports. An illustrative schematic of the traditional Wilkinson divider is shown in Fig. 1.

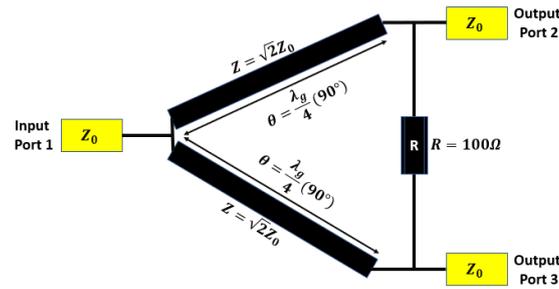


Fig. 1. The traditional Wilkinson power divider.

As discussed in the previous paragraph, the key to ultra-wideband design is to use an equivalent section of three different sized transmission lines using the stepped impedance method to replace the quarter-wave transformer link over the input and output ports, to achieve the desired specification at several different frequencies. Fig. 2 illustrates the quarter-wave transformer and its equivalent model using the stepped impedance techniques.

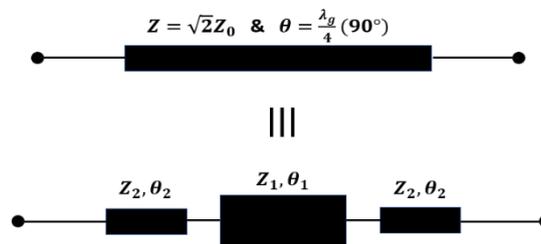


Fig. 2. Configuration of the conventional transformer and its equivalent model of the stepped impedance resonator.

The design of the considered power divider is based on the theoretical study of the conventional transformer and the stepped impedance resonator (SIR) by using the chain matrices of the ABCD parameters [21]. For the typical transformer which is depicted in Fig. 2, its ABCD chain matrix is given by equation (1).

$$M_{(\lambda_g/4)} = \begin{bmatrix} 0 & jZ \\ jY & 0 \end{bmatrix} \quad (1)$$

To validate the quarter wavelength microstrip line of the characteristic impedance Z_0 and the electrical length θ by its electrical model, the equations (2) and (3) are used to calculate its lumped elements (L and C) as follows:

$$L = \frac{Z}{\omega} \quad (2)$$

$$C = \frac{1}{Z\omega} \quad (3)$$

The stepped impedance resonator (SIR) shown in Fig. 2 consists of three cascaded microstrip transmission lines. Two symmetrical transmission lines are characterized by high impedance Z_2 and electrical length θ_2 , and one transmission line is characterized by low impedance Z_1 and electrical length θ_1 . The SIR of this resonator is analyzed by applying the ABCD matrix method. In our case, its

ABCD matrix is noted M_{SIR} , and equation 4 is the result of multiplying the ABCD matrix of the high-impedance transmission line noted M_2 , as expressed in equation 5, and the ABCD matrix of the low-impedance transmission line noted M_1 , as expressed in equation 6.

$$M_{SIR} = M_2 \cdot M_1 \cdot M_2 \quad (4)$$

$$M_{2(\text{High impedance})} = \begin{bmatrix} \cos \theta_2 & jZ_2 \sin \theta_2 \\ jY_2 \sin \theta_2 & \cos \theta_2 \end{bmatrix} \quad (5)$$

$$M_{1(\text{Low impedance})} = \begin{bmatrix} \cos \theta_1 & jZ_1 \sin \theta_1 \\ jY_1 \sin \theta_1 & \cos \theta_1 \end{bmatrix} \quad (6)$$

Whereas:

$$M_{SIR} = \begin{bmatrix} \cos \theta_2 & jZ_2 \sin \theta_2 \\ jY_2 \sin \theta_2 & \cos \theta_2 \end{bmatrix} \cdot \begin{bmatrix} \cos \theta_1 & jZ_1 \sin \theta_1 \\ jY_1 \sin \theta_1 & \cos \theta_1 \end{bmatrix} \cdot \begin{bmatrix} \cos \theta_2 & jZ_2 \sin \theta_2 \\ jY_2 \sin \theta_2 & \cos \theta_2 \end{bmatrix} \quad (7)$$

As a result, the equivalence of the stepped impedance resonator circuit to the quarter wavelength transmission line circuit leads to the system of equations (8) and (9).

$$\frac{Z_2}{Z_1} + \frac{Z_1}{Z_2} = \frac{2}{\tan \theta_1 \tan 2\theta_2} \quad (8)$$

$$\sin \theta_1 = \frac{Z - Z_2 \cos \theta_1 \left[\frac{\sin 2\theta_2}{2} + \cos^2 \theta_2 \right]}{Z_1 \frac{\sin 2\theta_2}{2} - \frac{Z_2^2}{Z_1} \sin^2 \theta_2} \quad (9)$$

As mentioned above, the goal is to design the novel power divider with operating broadband and minimized size. For the broadband criteria ($Z_2 \neq Z_1$), in our case, the impedance Z_2 is considered as high impedance and Z_1 as low impedance. As for the reduced size, the total length ($\theta_T = \theta_1 + 2\theta_2$) of the proposed resonator is less than the conventional transformer. In addition, the value of Z_1 , Z_2 , θ_1 , and θ_2 are determined in order to be physically realizable. The physical dimensions L_1 , L_2 , W_1 and W_2 of the proposed resonators are calculated using equations (10) and (11) [21].

$$W_i = \frac{8e^A}{e^{2A} - 2} \quad i = 1, 2 \quad , \quad (10)$$

$$L_i = \frac{c}{2\pi f_r \sqrt{\epsilon_r}} \theta_i \quad (11)$$

Where c is the speed of light and A is a parameter given by equation (12) [21]:

$$A = \frac{Z_i}{60} \sqrt{\frac{\epsilon_r + 2}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1} \left(0.23 + \frac{0.11}{\epsilon_r} \right) \quad , \quad (12)$$

These equations show the relationship between the electrical dimensions Z_1 , Z_2 , θ_1 and θ_2 obtained from the system of equations concerning the proposed stepped impedance resonator, the proposed substrate characteristic (h and ϵ_r), and the operating bandwidth center resonance frequency (f_r). All these parameters are obtained and listed in Table I.

TABLE I. VALUES FOR THE ELECTRICAL AND PHYSICAL PARAMETERS OF THE PROPOSED STEPPED IMPEDANCE RESONATOR

Electrical parameters		Physical parameters	
Z_1	62.52 Ω	W1	2 mm
θ_1	45.49 $^\circ$	L1	6 mm
Z_2	85.7 Ω	W2	1 mm
θ_2	36.9 $^\circ$	L2	5 mm

III. DESIGN AND DISCUSSION OF NUMERICAL RESULTS

After analyzing the various characteristic impedances and the electrical lengths of each transmission line of the proposed power divider, the results were verified using the schematic and integrated momentum method into the ADS simulator. The layout is plotted in Fig. 3.

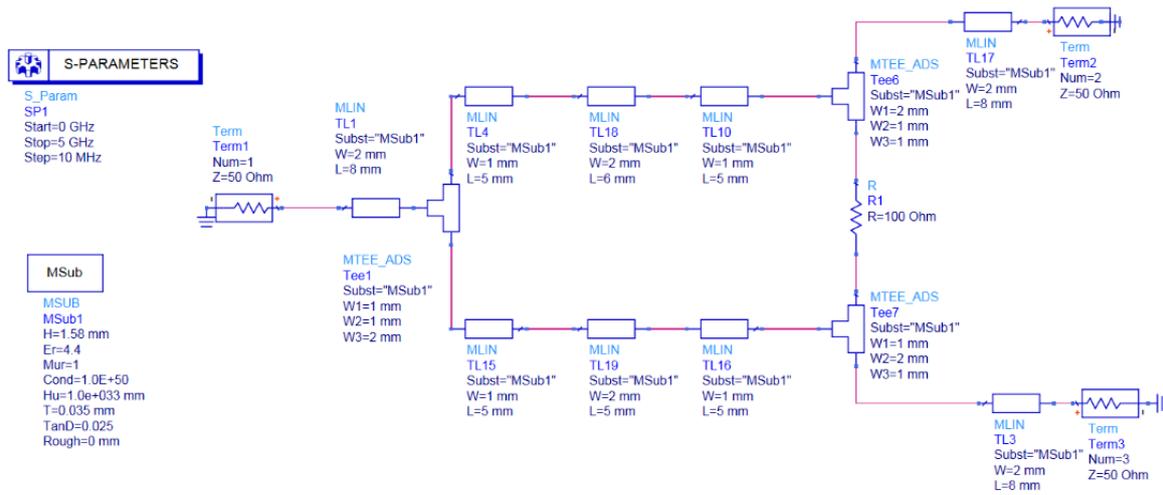


Fig. 3. Configuration of the proposed stepped impedance power divider/combiner - Schematic diagram.

In order to make better and more effective use of the internal surface area of the structure and to approximate the performance of the original structure developed through the analysis in the previous subsection, while avoiding overlaps, the final geometrical configuration of the stepped impedance transformer section was adjusted to optimize the surface area occupied as shown in Fig. 4. Eventually, the parameters were determined as follows: $L_1 = 6$ mm, $L_2 = 5$ mm, $W_1 = 2$ mm, $W_1 = 1$ mm

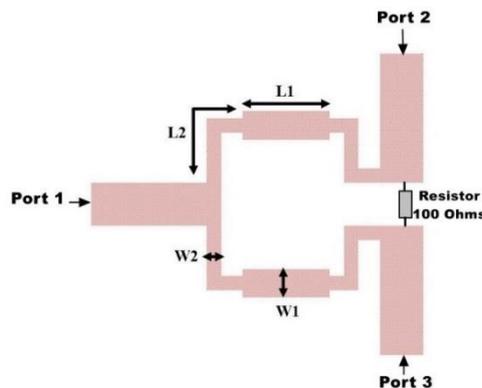


Fig. 4. Configuration of the proposed stepped impedance power divider/combiner - 2D layout.

Numerical results in terms of return loss at the three terminals demonstrate that the proposed structure provides a matching of up to 50 dB and an extremely wide frequency bandwidth of 4.3 GHz from 0.1 GHz to 5 GHz, as well as very good isolation of the output terminals (Ports 2 and 3) from 0.5 GHz to 4.8 GHz achieved through the 100 Ω resistor. In terms of input power transmitted to the two outputs, we can state that the structure can transmit power without losses over a bandwidth ranging from 0.2 GHz to 4.8 GHz. By combining these three parameters, we can conclude that the structure has an ultra-wide bandwidth from 1 GHz up to 4.2 GHz. The results are plotted in Fig. 5.

The phase shift must be the same across the outputs, which is also a crucial criterion for power dividers. For the proposed structure, we calculated the phase shift for frequencies ranging from 0 GHz to 5 GHz. The results are shown in Fig. 6 and demonstrate excellent and satisfactory performance.

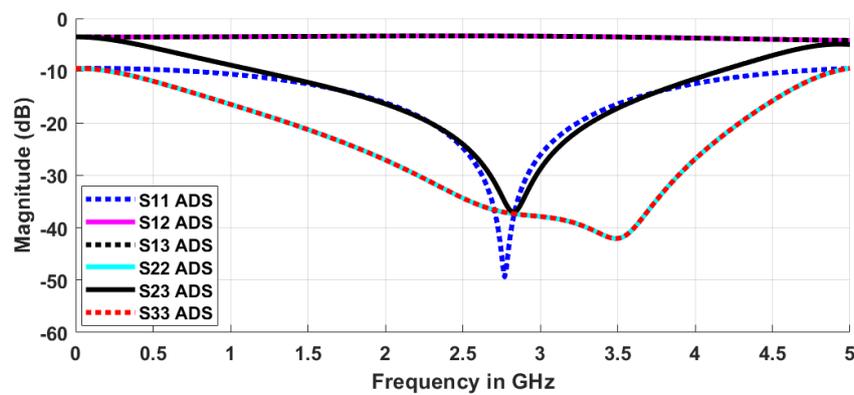


Fig. 5. Simulated S-parameters of the schematic model of the proposed Wilkinson power divider/combiner using ADS.

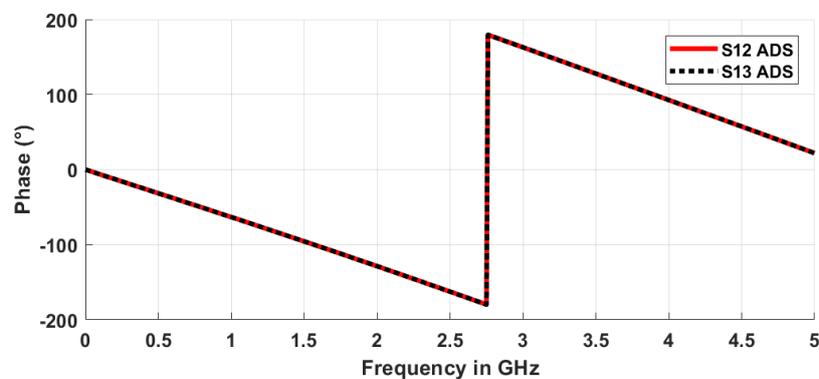


Fig. 6. Simulated phase vs frequency across the output ports of the proposed Wilkinson power divider/combiner using ADS.

Figures 7(a) and 7(b) show the surface current distributions at the 2.45 GHz center frequency allocated to ISM applications and at the 3.5 GHz frequency allocated to sub-6 GHz 5G applications. We can also see that both output ports receive the same current at the same time, which validates our approach.

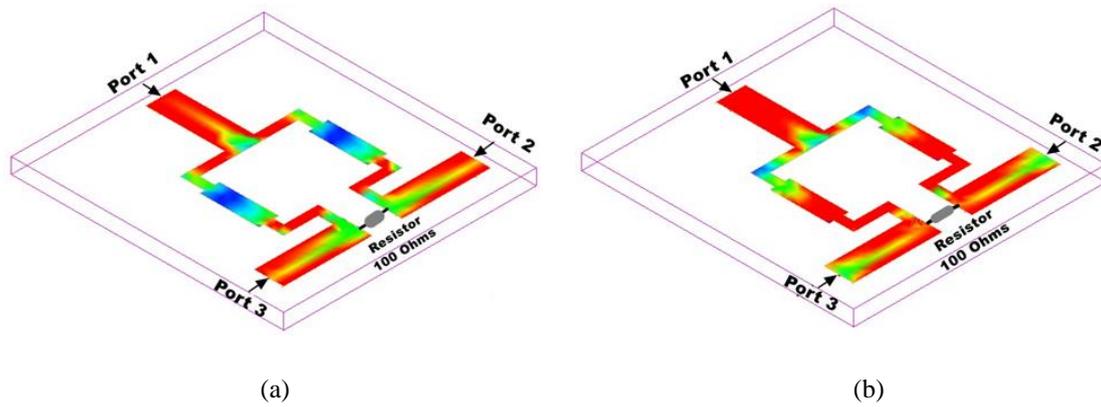


Fig. 7. Simulated current distribution of the proposed power divider/combiner (a) @ 2.45GHz (b) @ 3.5 GHz.

The equivalent electrical model of the proposed stepped impedance power divider/combiner using lumped elements (inductors and capacitors) is shown in Fig. 8. As can be seen from the figure, the model is symmetrical to the input port, each transmission line section of the 2D model has been substituted with the π -model of the transmission line, which typically comprises an inductor in series and two capacitors in parallel. The model is retrieved from the schematic configuration using equations (13) and (14).

$$L_i = \frac{Z_i \sin(\theta_i)}{\omega}, i = 1,2,3, \dots \quad (13)$$

$$C_i = \frac{1 - \cos(\theta_i)}{Z_i \omega \sin(\theta_i)}, i = 1,2,3, \dots \quad (14)$$

The values obtained for the reactive lumped elements are listed in Table II. The simulation results in terms of return losses, isolation between output terminals, and transmission of input power to the two output ports are shown in Fig. 9. As can be seen, the results of the electrical model based on lumped elements confirm those obtained by the schematic method under ADS.

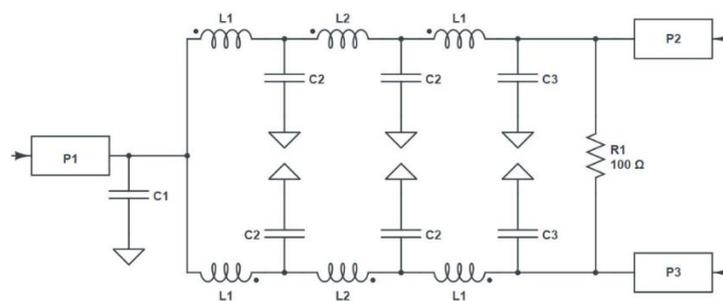


Fig. 8. Electrical equivalent model of the proposed stepped impedance power divider/combiner.

TABLE II. VALUES FOR THE LUMPED ELEMENTS OF THE ELECTRICAL MODEL

Lumped element	Value
C1	0.354 pF
C2	0.477 pF
C3	0.177 pF
L1	3.11 nH
L2	1.99 nH
R	100 Ω

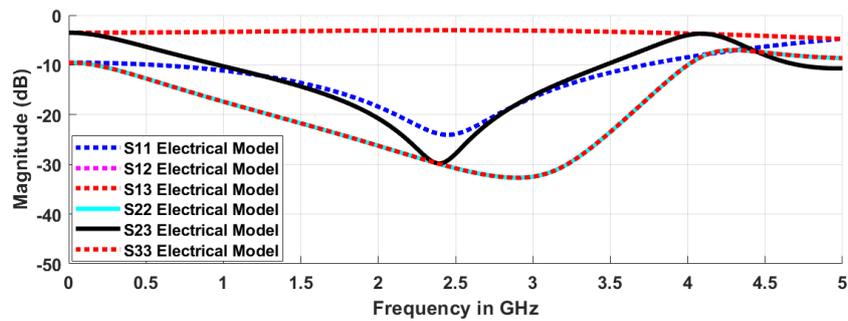


Fig. 9. Simulated S-parameters of the electrical model using lumped element.

As a further step towards validating the achieved findings and before proceeding to prototype manufacturing, we proceeded to verify the power divider/combiner using a 3D simulator incorporating the effect of the substrate and ground plane. The use of the two simulators, ADS and CST, offers complementary features and benefits. ADS can efficiently simulate the proposed power divider, which is a planar circuit, due to its Momentum method for electromagnetic analysis, which provides fast computation times. On the other hand, CST excels at handling complex 3D geometries and accurately capturing substrate effects due to its Finite Integration Technique. It can provide a more complete analysis, considering the limitations of ADS, particularly in handling complex geometries and substrate effects. Taking the strengths of both simulators into account, the goal is to improve the robustness and accuracy of the simulation results before prototyping. Fig. 10 gives the 3D layout in CST MS.

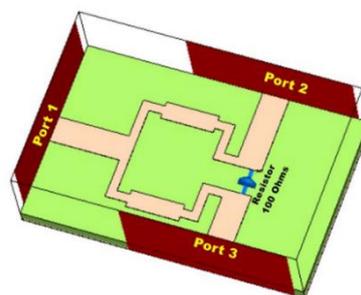


Fig. 10. The 3D layout of the proposed power divider using CST MS.

The numerical results evaluated through the CST MS simulator are plotted in Fig. 11. They are in close accordance with those obtained through the electrical and schematic models generated through ADS, although a slight difference is observed, due to the dissimilarity of the software algorithms used.

Due to the symmetry of the circuit, only coefficients S_{12} , S_{22} and S_{23} are listed, thereby providing the same listed parameters as S_{13} , S_{33} and S_{32} , respectively.

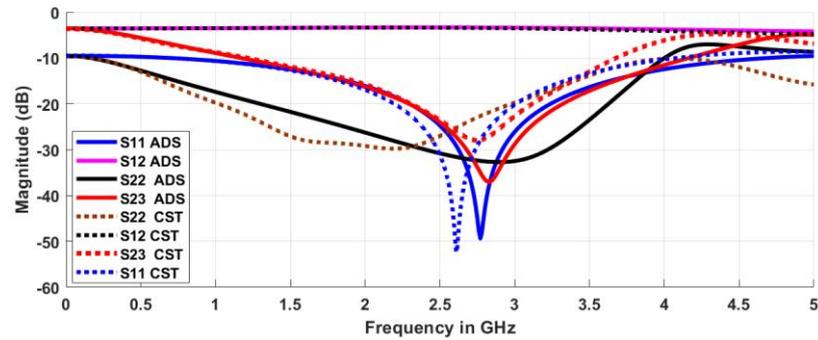


Fig. 11. Simulated S-parameters of the electrical model using lumped element using ADS and CST.

IV. PROTOTYPE AND MEASUREMENTS

After analysis and validation of the results through schematic and electromagnetic simulation, the prototype was fabricated on an Epoxy-FR4 substrate. A photograph of the prototype is given in Fig. 12 (a)-(b). As part of the validation process, the parameters of the proposed power divider/combiner were measured using an HP8719ES vector network analyzer. Fig. 12 (a) provides a photograph of the device under test to measure matching and transmission between input terminal P1 and output terminal P2. While Fig. 12 (b) displays the device under test for measuring matching and isolation on both output ports P2 and P3.

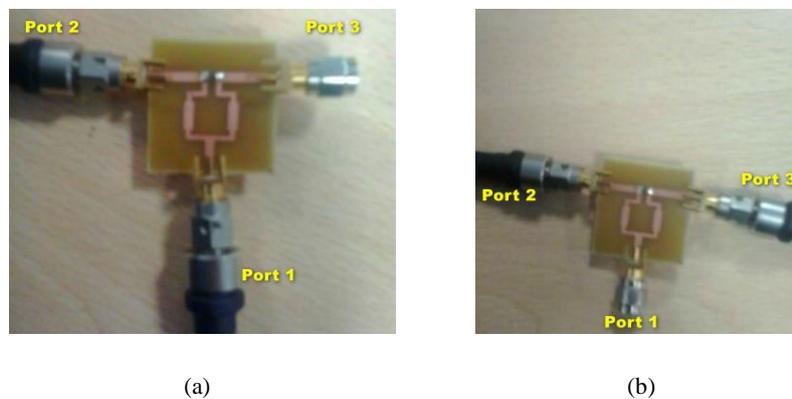


Fig. 12. The realized prototype of the proposed broadband stepped impedance power divider/combiner.

The measured results are presented in Fig. 13 and show good conformity those obtained through simulation, except for isolation: the band was reduced at low frequencies, due to poor port connection during the measurement process. Note that the S_{21} experimental transmission coefficient throughout the 1.2 GHz to 3.7 GHz band fluctuates between -3.5 dB and -4.3 dB. As can be deduced from the results reported above, the implementation of our approach has been confirmed.

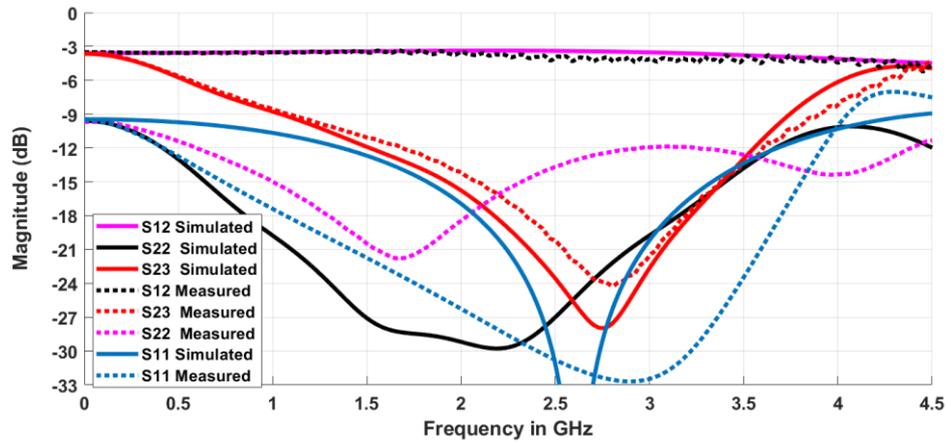


Fig. 13. The measured VS simulated S-parameters of the realized prototype of the proposed broadband stepped impedance power divider/combiner.

The developed power divider/combiner was compared against other recently published work in terms of bandwidth, size reduction rate, and prototype fabrication method complexity. As highlighted in Table III, the proposed structure achieves a reduction of almost 75% compared to the conventional Wilkinson divider, while other work achieves a maximum reduction of 61%. It is worth noting that the typical divider was designed based on the Wilkinson model [22], uses quarter-wavelength transmission lines, and occupies a size of 51.93 mm x 55 mm and has a low fractional bandwidth 1.2 GHz to 3 GHz. In addition, it exhibits undesirable harmonics. On the other hand, the proposed structure achieves a bandwidth of 3.5 GHz ranging from 1.2 GHz to 3.7 GHz, which represents the highest bandwidth achieved in the comparative table, excluding the circuit published in [28], but in terms of the fabrication method, the proposed solution is simple to produce and offers low cost.

TABLE III. COMPARISON OF THE PROPOSED STRUCTURE WITH RECENTLY PUBLISHED RELATED WORK

References	Operating Bandwidth (GHz)	Size Reduction	Methods	Prototyping Complexity
[22]	[1.2-3.6]	No size reduction	Conventional Transmission Lines Sections	Simple
[23]	[1-3.2]	44%	Resonator Cells	Complex and costly
[24]	[1-3.1]	36.5%	Open Stubs	Simple and low cost
[25]	[1.5-2.6]	55%	Resonator Cells	Complex and costly
[26]	[2.1-3.7]	31 %	Short and open stubs	average
[27]	[2.4-2.6]	70%	Lumped Elements & Resonator Cells	Complex and costly
[28]	[3-8]	61%	DGS Floating conductor	average
[29]	[1.7- 4.64]	No size reduction	Stepped Impedance Resonators SIRs	Simple and low cost
[30]	[1.2- 3.3]	34.5%	EBG Cells	Complex and costly
Proposed work	[1.2-3.7]	75%	Stepped Impedance Resonators SIRs	Simple and low cost

V. CONCLUSION

This study proposed to design a new Wilkinson power divider/combiner structure based on the stepped impedance resonator method to extend its bandwidth to cover a wide range of wireless applications. The stepped impedance resonator has been redesigned to minimize the size of the final structure. First, the basic concepts and theories needed for the general design of power dividers/combiners based on ABCD transfer matrices were presented. This was followed by a proposal for a divider/combiner that replaces the conventional quarter-wave transformer using an SIR resonator. The performance of this divider, particularly in terms of impedance matching, isolation, and transmission, was validated using a prototype and compared to related research recently published in terms of size, bandwidth, and complexity of implementation. The results obtained showed that the proposed structure has an ultra-wide bandwidth and a small size, making it an attractive alternative for wireless applications, particularly 5G technology.

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