Preparation and Characterization of CdO/In$_6$Se$_7$ Thin Film Transistors

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In this study, the design and characterization of CdO/InSe thin film transistors (TFT) that are grown onto Au substrates are investigated. The devices are also subjected to a vacuum annealing process at 300 ºC to enhance the structure and electrical performance. It was observed that the growth of polycrystalline monoclinic In$_6$Se$_7$ phase of InSe is preferred at this annealing temperature when coated onto Au/CdO substrates. Electrically, noisy negative capacitance effect accompanied with resonance-antiresonance phenomena is observed in the capacitance spectra of the as prepared TFT devices. The annealing of the TFT devices reduced the noise in the capacitance, conductance, impedance, and reflection coefficient and return loss spectral responses. The heat treated TFT devices displayed low bandpass, high bandpass and bandstop filter characteristics in the studied frequency domain (0.01-1.80 GHz) indicating the applicability of these devices as radio wave-microwave resonators.

Keywords: *CdO/InSe, annealing, thin film transistor, band filter.*

1. Introduction

Cadmium oxide substrates are promising layers which find many optoelectronic applications. The CdO substrates are employed for the third and triplet photon generation[1]. Recently, dielectric- loaded waveguides is designed onto CdO transparent substrates for this purpose. These waveguides are nominated as platforms for integrated triplet photon generation which can be used for on-chip wavelength conversion, MIR up-conversion photodetection, and quantum signal processing[1]. CdO substrates are also used for gas sensing[2]. A sensitivity of 20-33% to oxygen gas in the temperature range of 32-200 ºC is reported. In addition, CdO substrates are regarded as good layers for the production of photodiodes which can perform well in the visible range of light[3].

On the other hand, indium selenide thin films coated onto various dielectric substrates are reported to be beneficial for the production of thin film transistors which can handle multi-issue at a time[4,5]. As thin film transistors InSe processes high gain and short response time which make it attractive for the fabrication of photodetectors and micro-light emitting diode displays[5]. In$_2$Se$_3$ is also used in the fabrication of nonvolatile memory devices[6]. α-In$_2$Se$_3$/WSe$_2$ vertical heterojunction devices are mentioned exhibiting switchable diode characteristics and nonvolatile memory phenomenon. The photodiodes displayed a high on/off ratio at small switching voltages.

The features of the CdO substrates and the wide range of applications of InSe motivated us to bring these two materials together to form a heterojunction device. As the work function ($q\phi$) of CdO being 3.45 eV[6] is less than the work function of Au (5.34 eV), the Au/p-CdO form an ohmic interface. Similarly the ohmic contact to n-InSe layer is achieved by using ytterbium ($q\phi = 2.54\,eV$) pads. The Au/CdO/InSe/Yb thin film transistor (TFT) devices is tested as passive mode device responsive to ac signals. Particularly, here in this work, the TFT devices is structurally, morphologically and electrically evaluated by means of X-ray diffraction, scanning electron microscopy and impedance spectroscopy techniques. An annealing process is also performed to enhance the electrical performance of the TFT transistors.

2. Experimental Details

Au, Yb, CdO and InSe thin films are prepared by the thermal evaporation technique under vacuum pressure of 10^{-5} mbar. The respective source materials were high purity gold wire (99.97%), ytterbium lumps (99.99%), CdO powders (99.99%) and $\alpha - In_2Se_3$ (99.99%) poly-crystals. The first Au layer (1.0 µm thick) was coated onto ultrasonically and chemically cleaned glass substrates. The resulting Au metal films were used as substrate to grow CdO films (0.5 µm thick). The Au/CdO films were coated with InSe layer of thickness of 0.5 µm. The resulting Au/CdO/InSe films are masked and coated with pad shaped Yb films. The area of each pad was $3.14 \times 10^{-2}\,cm^{-2}$. The geometrical design of the device is shown in the inset of Figure 1. The films thicknesses were monitored with Inficon STM-2 thickness monitor attached to the system. The produced Au/CdO/InSe/Yb films were heat treated at 300 ºC for one hour under vacuum pressure of 10^{-5} mbar. The heating rate before reaching the targeted temperature was ~20 ºC/min. The X-ray diffraction was recorded with the help of Miniflex-600 X-ray diffraction unit at scanning speed of 0.1º/min. The surface morphology was scanned using COXEM 200 SEM system. The impedance

spectroscopy was collected between Au (base) and top Yb contact using Agilent 4291B 0.01-1.80 GHz impedance analyzer. The connections to the 16453A dielectric material test fixture were made by AP-7 connector attached to the analyzer.

3. Results and Discussion

The X-ray diffraction patterns for the Au, as prepared Au/CdO/InSe (ACI) and annealed Au/CdO/InSe thin films are shown in Figure 1. The heterojunction ACI devices were annealed at 300 ℃ for one hour in a vacuum media of 10^{-5} mbar. It is clear from the figure that the as prepared heterojunction devices exhibit amorphous nature of growth owing to the appearance of no extra peaks other than that of gold substrate. The analysis of the peaks which are reflected from the gold thin film substrates indicated the existence of the face centered cubic structure with best plane orientation along the (111) direction. The lattice parameters of the as prepared Au unit cell is found to be $a = b = c = 4.06$ Å. The reflection peaks of the Au substrates also included one peak that is assigned to orthorhombic Au_2O_3 (a=12.827 Å,=10.520 Å, c=4.038 Å[7]). On the other hand, as displayed in Figure 1, annealing the samples at 300 ℃, induced the crystallization process in the ACI heterojunction devices. Namely, new peaks other than that of gold appear in the XRD patterns. Our theoretical investigations on the polycrystalline phases of InSe and CdO using "Crystdiff" software packages have shown that none of these peaks can be assigned to the cubic CdO ($a = 4.696$ Å)[8]. Excluding the Au peaks as they already exist in the XRD patterns, none of the peaks can also be assigned to the hexagonal CdO which is mentioned displaying peaks at 33.31° (111), 38.40° (200) and 55.65° (220)[9]. Trails to index the experimental data of the annealed ACI sample assuming the growth of hexagonal $(\alpha, \beta, \gamma) - In_2Se_3$[10,11], orthorhombic In_4Se_3[11] and monoclinic In_6Se_7 has shown that all the experimentally observed peaks can be assigned to the monoclinic In_6Se_7 phase of indium selenide[12]. The lattice parameters of the obtained monoclinic unit cell are found to be $a = 9.433$ Å, $b = 4.064$ Å, $c = 17.663$ Å and $\beta = 100.92°$. The lattice paropameters are consistent with literature data[12] and the crystallography open database (COD NO: 8104059). The unit cell of this structural phase is demonstrated with the help of "Crystalmaker" software packages in Figure 2a. As illustrated, the unit cell is composed of two separate sections of cubic close-packed arrays of selenium atoms with indium atoms in octahedral coordination. The two parts of the cell are located across the center and end sections of the unit cell and may be brought into the same orientation direction through rotating one of them by 61 ° about the [010] direction. The calculated bond lengths with the help of the "crystalmaker" software packages vary in the range of 2.66 Å (In4-Se2) to 2.76 Å (In1-In2).

Figure 2b and c show the surface morphology of the as prepared and annealed Au/CdO/InSe heterojunction devices, respectively. While the enlargement of 20,000 times displays randomly distributed circularly shaped grains of average sizes of ~150 nm, the same enlargement of the annealed samples display mostly randomly distributed rectangular grains of sizes of 120 nm. The density of grains on the surface is higher for the as prepared thin film transistors than those which were annealed at 300 ℃ for one hour. It is mentioned that the size of recrystallized grain is identified by both the nucleation and growth rates. For non-oriented electrical steels, it was found that during the annealing process, if the heating process is fast, less recovery take place[13]. This leads to the storage of extra energy in the crystallites before the recrystallization is initiated. Higher stored energy increases the nucleation rate faster than the growth rate. For this reason, the annealing by fast heating forces the formation of smaller grain sizes than that of slow heating[12]. Other studies accounted the decrease in the grain size upon annealing to the quantum size effect (QSE)[14]. It was shown that the growth dynamics and morphology of grains (islands on thin films) can be well controlled through the quantum size effects defined by
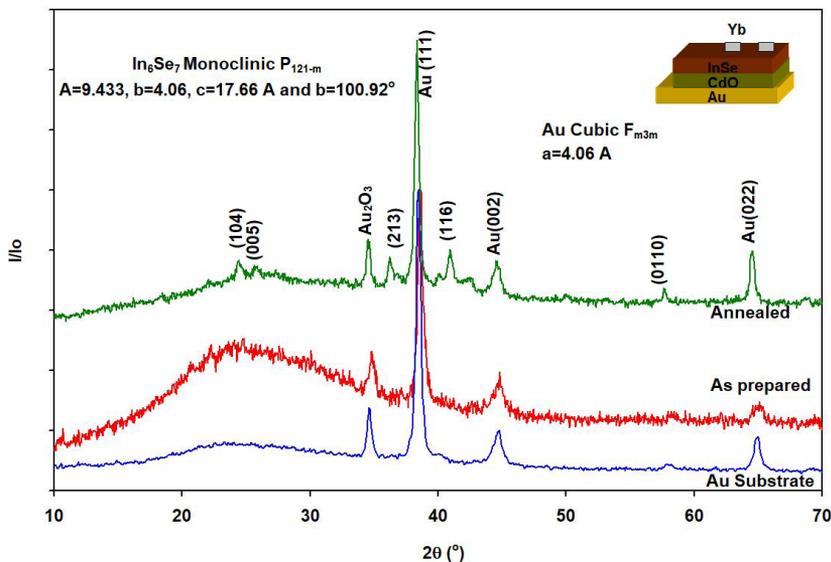

Figure 1. the X-ray diffraction patterns for Au, as prepared Au/CdO/InSe and for the annealed Au/CdO/InSe thin film transistors. The inset shows the geometrical design of the device.
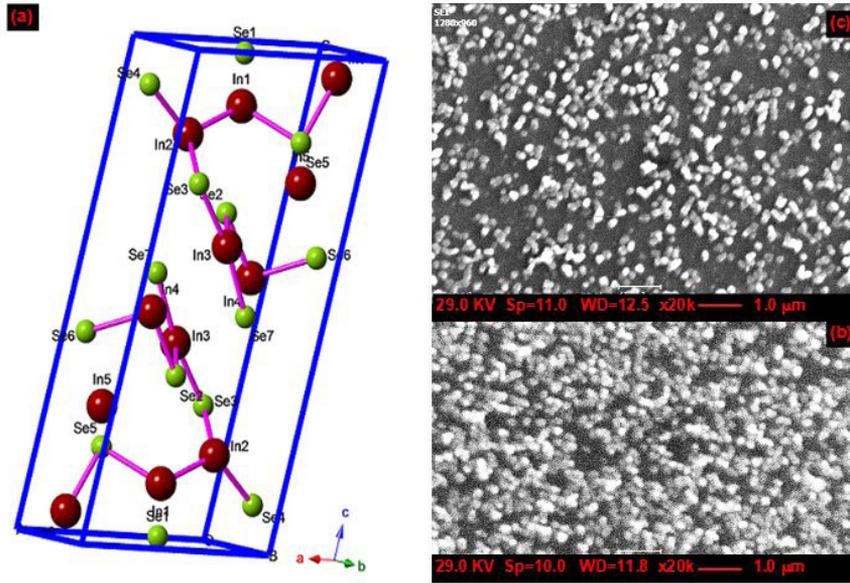
Figure 2. (a) the schematics of In$_6$S$_7$ crystals which are grown by the annealing of InSe onto CdO substrates and the scanning electron microscopy images for the (a) as prepared and (b) annealed Au/CdO/InSe thin film transistors.
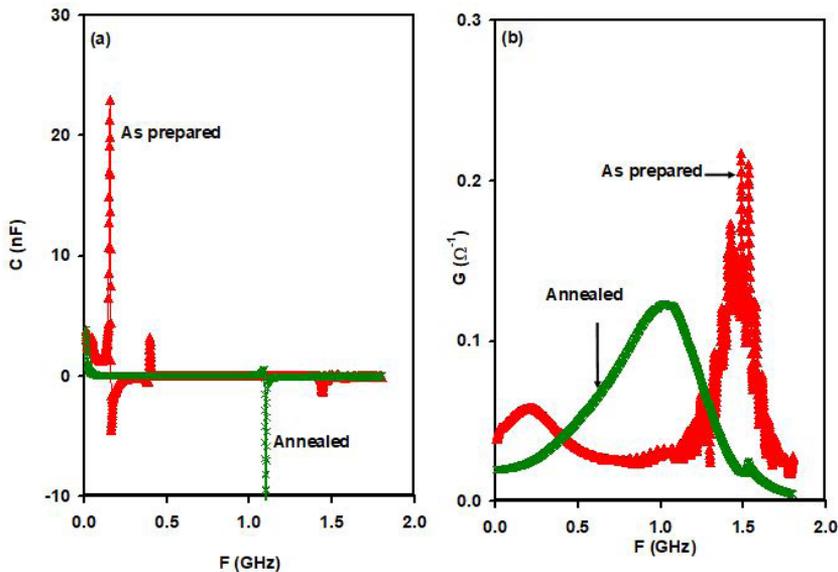

Figure 3. (a) the capacitance and (b) conductance spectra for the Au/CdO/InSe thin film transistors before and after annealing.

the island thicknesses and the interplay with the classical forces[15]. The QSEs are mentioned predominating both the formation and stability of thin films at nanoscale levels. On the other hand, free energy costs from steps provide the usual "classical" driving force to smoothen the film's surface. The restrictions of growth of grains along particular plane direction, forces quantization of this direction, as a result the only possible energy stabilization which is gained by annealing is achieved via grain growth along the remaining two directions.

Figure 3a and b show the heat treatment effects on the capacitance (C) and conductance (G) spectra for the

Au/CdO/InSe/Yb devices. It is clear from the Figure 3a that the capacitance of the as prepared Au/CdO/InSe/Yb thin film transistors exhibit resonance peaks at three different critical frequency values. Namely, one may observe strong resonance peaks at 0.15 GHz followed by antiresonance peak at 0.16 GHz. The second resonance peak appears at critical frequency value of 0.40 GHz. The third antiresonance peak is centered at 1.44 GHz. Annealing the devices at 300 °C for one hour leads to the disappearance of these peaks and force the capacitance spectra to exhibit one antiresonance peak centered at 1.10 GHz. While the capacitance spectra of the as prepared ACI devices fluctuates exhibiting positive

and negative values, the capacitance spectra of the annealed devices remain positive for all signal frequencies less than 1.10 GHz and negative for all frequency values larger than 1.10 GHz. Negative capacitance effect is ascribed to many reasons like minority carrier injections caused by accumulation of minority carriers at the grain boundaries[16]. The dense and random distribution of the grains in the as prepared samples that appears in Figure 2b could account for the random fluctuations in the capacitance spectra. Namely, the random distribution and different sizes of grains causes narrow and wide energy barriers at the grain boundaries. This leads to potential barriers of different depths and widths. Each of these barriers behaves as charge accumulation layers that differs in character than the other resulting in a random responses of capacitance to ac signals as observed. The crystallization process and the less dense grains that are achieved by the annealing of the devices (Figure 2c) may be regarded as a reason for the enhanced behavior of capacitance spectra. The negative capacitance effect can also be attributed to the carrier capture and emission at the CdO/InSe interface states. The process of capture and emission through the interface states were previously observed for InN/GaAs heterojunctions[17]. On the other hand, the existence of resonance-antiresonance peaks in the capacitance spectra of Au/CdO/InSe/Yb TFTs could be assigned to the oscillations of electric dipoles with or against the propagating ac signals[18]. As the signal propagation is limited by the plasmon frequency of the dielectric media, the formation of the heterojunction from two different materials should lead to at least two plasmon frequencies arising from electrons at one side and from holes at the other side. The plasmon frequencies force the dipoles to exhibit resonance when the signal frequency values approaches that of plasmon[18].

Figure 3b illustrates the annealing effects on the conductance spectra of the studied Au/CdO/InSe/Yb devices. It is clear from the figure that the conductance of the as prepared samples exhibits one local and one absolute maxima at 0.25 and 1.49 GHz, respectively. The shape of the $G-f$ variation in the as prepared devices comprises noisy signals. Annealing the devices leads to more stable $G-f$ variation, caused disappearance of the local peak, shifts the maxima to 1.09 GHz and make the peak width broader. The increase in the values of the conductance with increasing signal frequency up to a critical frequency value which is followed by a decrease in the conductance value with increasing frequency is attributed to the presence of more than one conduction mechanism in the devices. These trends of variations of the conductance spectra are assigned to the combined current conduction of tunneling and correlated barriers hopping (CBH) mechanisms[17]. Similar to our observation for ACI samples, the conductivity spectra of CdS/Sb$_2$Te$_3$ heterojunction devices have shown maximum peak at 0.26 GHz. The behavior of the conductivity was ascribed to the tunneling in the narrow depletion width and to the CBH owing to the hopping of charge carriers between defect centers over the potential barrier[17]. As the crystalline phase of InSe which is achieved by the annealing process exhibit lower surface defect density than the amorphous films, one may expect modifications in the current conduction mechanism which leads to the observed behavior of conductance. Other heterojunction devices which exhibit similar conductance spectra assigned this behavior to the same current conduction mechanisms[19]. Namely, the alternating current transports mechanism in TiO$_2$/ITO/ZnO:Al/p-Si structure is assigned the response of a thermally activated traps to the ac signal frequency[19]. The conduction is observed to be governed by the correlated barrier hopping mechanism involving two distinct energy levels at low frequencies. In the high frequency region, conduction is dominated by the overlapping large-polaron tunneling mechanism[19].

The total effect of resistive, inductive and capacitive parts is better observed from the impedance (Z) spectra which is illustrated in Figure 4a. The impedance spectra of the as prepared TFT devices display a broadened peaks centered at 0.49 GHz. It also shows an increasing trend of variation in the frequency domain of 1.50-1.80 GHz.
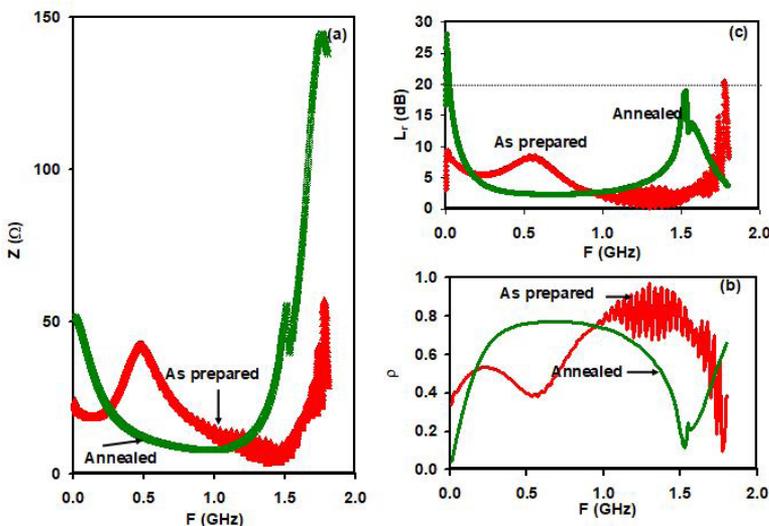

Figure 4. (a) the impedance (b) the reflection coefficient and (c) the return loss spectra for the Au/CdO/InSe thin film transistors before and after annealing.

The annealing of the ACI devices display a different style of variation. Namely, the impedance decreases with increasing frequency in the frequency domain of 0.01-1.05 GHz. It, then, sharply increases with increasing frequency. It increased from 7.8 Ω at 1.05 GHz to 143.0 Ω at 1.77 GHz. The frequency based switching in the impedance value from low to high impedance modes is an indication of the band filtering property. These signs are assured by calculating the magnitude of the reflection coefficient ($\rho = \dfrac{Z_{ACI} - Z_{source}}{Z_{ACI} + Z_{source}}$)[20] of the devices before and after annealing. The calculated reflection coefficient spectra are shown in Figure 4b. It represents the quality of the impedance match between the source of the signal and the measured device under study. ρ is small for good matches. It takes values from −1 for shorts, is zero for perfect matches and reaches +1 for open loads. As the figure shows, the as prepared ACI devices display one local and one absolute minima at signal frequency values of 0.58 and 1.78 GHz, respectively. The $\rho - F$ signal is very noisy and distorted. Annealing the ACI devices at 300 ºC for one hour highly affected the behavior of ρ spectra. Particularly, it increases from 0.04 at 0.01 GHz to 0.75 at 0.47 GHz. Then, it tends to remain constant in the frequency domain of 0.47-0.89 GHz. Thereafter, the reflection coefficient spectra sharply decrease with increasing signal frequency exhibiting a minima of 0.13 at 1.53 GHz. While the region of 0.01-0.47 GHz show a high pass filter, the 0.47-0.89 GHz region represent a band pass filter. The third region (0.89-1.80 GHz) indicate features of band stop filter. The quality of these filters can be understood from the calculations of the return loss spectra ($L_r = -20 log (\rho)$ [20]). The higher the absolute value of the return loss, the better the match, the more accurate the data transfer. L_r is a measure of the power that is not absorbed by the load and is therefore returned to the source. Large absolute values of L_r (greater than |20| dB) indicate a good match. The calculated return loss spectra are shown in Figure 4c. It is clear from the figure that while the as prepared heterojunction ACI devices hardly reaches the standard values (~20 dB), the annealing enhances the return loss values significantly in the high pass mode (0.01-0.47 GHz). It also shows acceptable values[21,22] of L_r at the notch frequency (1.53 GHz) while operating in the band stop mode (0.89-1.80 GHz).

The novelty of the current study lay in finding a procedure to improve the performance of the proposed band pass/stop filters and microwave cavities that are made of Au/CdO/InSe/Yb thin films. The annealing of the devices in a vacuum media at high temperature for one hour improved the response to the propagating ac signal in the devices. Noise is remarkably reduced and negative capacitance effect that is needed for parasitic capacitance cancellation become more pronounced. In addition, better matches between the propagating signals and devices is achieved by this procedure.

4. Conclusions

In the current study, we have shown that the annealing of Au/CdO/InSe/Yb thin film transistors at 300 ºC in a vacuum atmosphere (10^{-5} mbar) can enhance the performance of the devices significantly. Particularly, the success of the annealing process to transfer the amorphous structure of InSe to the monoclinic polycrystalline phase is accompanied with improvements in the electrical properties. The annealing reduced the signal distortion, enhanced the negative capacitance effect at high frequencies and forced the devices to exhibit band pass/stop features. The annealed devices displayed return loss value that exceeds the standards in the megahertz frequency domain where the device behaves as high band pass filters and, approximately, reaches standards in the Gigahertz frequency domain where the device behaves as band stop filters. The annealing process makes the Au/CdO/InSe/Yb devices more appropriate for use as microwave cavities.

5. Acknowledgements

6. References

1. Huang T, Pan J, Cheng Z, Song C, Wang J, Shao X, et al. Photon–Plasmon Coupling for Fundamental-Mode Phase-Matched Third Harmonic and Triplet Photon Generation. J Lightwave Technol. 2018;36(18):3892-7.

2. Rajput JK, Pathak TK, Kumar V, Swart HC, Purohit LP. Tailoring and optimization of optical properties of CdO thin films for gas sensing applications. Physica B. 2018;535:314-8.

3. Dugan S, Koç MM, Coşkun B. Structural, electrical and optical characterization of Mn doped CdO photodiodes. J Mol Struct. 2020;1202:127235.

4. Wang H, Liu Q, Feng X, Deng A, Dai J, Liu Z. P- 9.6:ultrathin Indium selenide (In2Se3) thin films and field- effect transistors for active matrix addressable micro- LEDs. International Conference on Display Technology. 2018;49(S1):677-8.

5. Yang H, Xiao M, Cui Y, Pan L, Zhao K, Wei Z. Nonvolatile memristor based on heterostructure of 2D room-temperature ferroelectric α-In 2 Se 3 and WSe2. Sci China Inf Sci. 2019;62(12):220404.

6. Bagal VS, Patil GP, Deore AB, Suryawanshi SR, Late DJ, More MA, et al. Surface modification of aligned CdO nanosheets and their enhanced field emission properties. RSC Advances. 2016;6(47):41261-7.

7. Shi H, Asahi R, Stampfl C. Properties of the gold oxides Au2O3 and Au2O: first-principles investigation. Phys Rev B Condens Matter Mater Phys. 2007;75(20):205125. http://dx.doi.org/10.1103/PhysRevB.75.205125.

8. Bakke JR, Hägglund C, Jung HJ, Sinclair R, Bent SF. Atomic layer deposition of CdO and CdxZn1− xO films. Mater Chem Phys. 2013;140(2-3):465-71.

9. Xu D, Guan M, Xu Q, Guo Y, Wang Y. Ethanol sensor of CdO/Al2O3/CeO2 obtained from Ce-doped layered double hydroxides with high response and selectivity. Funct Mater Lett (Singap). 2013;6(03):1350035.

10. Madelung O. Semiconductors: data handbook. Heidelberg: Springer Science & Business Media Berlin; 2012.

11. Omareya OA, Qasrawi AF, Al Garni SE. Effect of Au nanosandwiching on the structural, optical and dielectric properties of the as prepared and annealed InSe thin films. Physica B. 2017;520:57-64.

12. Hogg JHC. The crystal structure of In6Se7. Acta Crystallogr B. 1971;27(8):1630-4.

13. Park J-T, Szpunar JA, Cha S-Y. Effect of heating rate on the development of annealing texture in nonoriented electrical steels. ISIJ Int. 2003;43(10):1611-4.

14. Sathyamoorthy R, Sharmila C, Natarajan K, Velumani S. Influence of annealing on structural and optical properties of Zn_3P_2 thin films. Mater Charact. 2007;58(8-9):745-9.

15. Li SC, Ma X, Jia JF, Zhang YF, Chen D, Niu Q, et al. Influence of quantum size effects on Pb island growth and diffusion barrier oscillations. Phys Rev B. 2006;74(7):075410.

16. Wang K, Shen WZ, Yang HF. Capacitance characteristics in PbSrSe thin films. Appl Surf Sci. 2003;217(1-4):100-7.

17. Pan W, Shen WZ. Electrical properties in hexagonal InN thin films. In: Conference Series-Institute of Physics; 2005; Philadelphia. Proceedings. Philadelphia: Institute of Physics; 2005. vol. 184, p. 259.

18. Khusayfan NM, Qasrawi AF, Khanfar HK. Design and electrical performance of CdS/Sb2Te3 tunneling heterojunction devices. Mater Res Express. 2018;5(2):026303.

19. Nouiri M, El Mir L. Effect of impedance relaxation in conductance mechanisms in TiO2/ITO/ZnO: Al/p-Si heterostructure. J Electron Mater. 2018;47(5):3018-25.

20. Pozar DM. Microwave engineering. New York: Wiley; 2012.

21. Al-Shalaby NA, Gaber SM. Design of dielectric resonator band stop/band pass filters. Appl Comput Electromagn Soc J. 2019;38(8)

22. Moitra S, Dey R. Design of dual band and Tri-band Bandpass Filter (BPF) with Improved inter-band isolation using DGS integrated coupled microstrip lines structures. Wirel Pers Commun. 2019;110:1-12.