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A Balanced-to-Single-Ended Wilkinson Power Divider

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***Abstract*—A balanced-to-single-ended (BTSE) Wilkinson power divider of planar microstrip structure is proposed in this paper. It has a balanced input and two single-ended outputs. Cascade of a balun and a conventional power divider can be replaced by this proposed structure. Based on the theory of mixed-mode S parameters and the admittance matrix method, the critical parameters are determined. The four-port network is analyzed by simplifying it to two-port network with other ports matched at the central frequency. Then the key parameters are derived and the impact of a freely selected variable on the bandwidth is also discussed. An example of 2.4GHz BTSE power divider is designed. The simulated and measured results show the effectiveness of the method: differential-mode transmissions are better than -3.25dB, common-mode transmissions are lower than -28.6dB, common-mode return loss is -0.10dB, differential-mode return loss and isolation is lower than -23.7dB. While the operating bandwidth is 20%.**

***Index Terms*—**balanced circuit; power divider; mixed-mode S-matrix

I. INTRODUCTION

Balanced RF circuits have more advantages than single-ended ones. The most important advantage is the ability of anti common-mode interference. As power divider is an important microwave/millimeter wave passive device, scholars have made a deep research on balanced power dividers [1-7].In [1], a wide band miniature balanced power divider is designed with the coupled lines. Then a balanced Wilkinson power divider with microstrip structure was presented [2], it contains four lumped resistors which affect the performance when working at high frequency. Later, some scholars improved the structure by using two resistors [3]. Further in [4], the lumped resistors were reduced to one. By using half-mode substrate integrated waveguide (SIW) structure, a balanced symmetric Gysel power divider is designed [5]. Also, balanced Gysel power divider with arbitrary power division ratio [6] and dual-band balanced Wilkinson power divider [7] are designed.

As mentioned above, these studies are all about the balanced-to-balanced (BTB) power divider, but in some modern practical applications, it may demand a power divider which contains both single-ended port and balanced port, such as when the signals received by a balanced antenna need to be processed by single-ended receivers [8] or when the differential power amplifier need to be connected

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to a single-ended antennas to work in a radar system effectively [9]. Research in this area is relatively few. A BTSE power divider is designed with double-side structure [10], which brings inconvenience to practical application. [11] proposed a BTSE power divider with filtering function, however, the operating bandwidth of it is less than 7%.

In this paper, the relationship between mixed-mode S-matrix and traditional S-matrix of the four port network of the proposed power divider is analyzed and derived, then a transformation is introduced to simplify the design process. At last, based on the mixed-mode S parameters theory and the admittance matrix method of the two-port balanced network, a new BTSE power divider with planar microstrip structure is proposed. And its performances are demonstrated by the simulated and measured results. The impact of a freely selected variable on the bandwidth is also discussed.

II. ANALYSIS AND DERIVATION OF KEY PARAMETERS

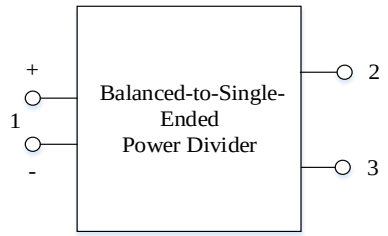

Fig. 1. Schematic diagram of a three port BTSE power divider

As shown in Fig.1, a three port BTSE power divider transmit the input signal from balanced port 1 to single-ended ports 2 and 3. In the research of balanced circuit, we often use mixed-mode S-matrix to replace the traditional S-matrix. Its mixed-mode S-matrix is

$$[S_M]=\begin{bmatrix} S_{DD11} & S_{DC11} & S_{DS12} & S_{DS13} \\ S_{CD11} & S_{CC11} & S_{CS12} & S_{CS13} \\ S_{SD21} & S_{SC21} & S_{SS22} & S_{SS23} \\ S_{SD31} & S_{SC31} & S_{SS32} & S_{SS33} \end{bmatrix} = \begin{bmatrix} S_{DD} & S_{DC} & S_{DS} \\ S_{CD} & S_{CC} & S_{CS} \\ S_{SD} & S_{SC} & S_{SS} \end{bmatrix} \tag{1}$$

In this matrix, S_{XYij} means the S-parameter when port j is in Y mode excitation and port i is in X mode response, where X, Y are corresponding to differential mode (D), common mode (C) or single-ended mode (S), while i, j are corresponding to port 1, port 2 or 3. At the same time, S_{XY} represents the corresponding matrix block.

Typically, the parameters should meet the following conditions:

1) The power divider should be reciprocal, so its mixed-mode S-matrix is symmetric ($S_{XYij}=S_{YXji}$);

2) Each port should be matched to the differential signal, at the same time, single ports are also matched ($S_{DDii}=0$ and $S_{SSii}=0$);

3) The input common mode noise should be fully reflected, with no mutual conversion between the common mode signal and differential mode signal ($|S_{CCii}|=1$ and $|S_{CDii}|=|S_{DCii}|=|S_{CDij}|=|S_{DCij}|=0$);

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4) The output ports should be isolated from each other($|S_{SS23}|=0$ and $|S_{SS32}|=0$).

According to these, the desired mixed-mode S-matrix of the power divider with equal power division will be:

$$[S_M]=\begin{bmatrix} 0 & 0 & \sqrt{2}e^{-j\varphi_1}/2 & \sqrt{2}e^{-j\varphi_2}/2 \\ 0 & e^{-j\varphi_3} & 0 & 0 \\ \sqrt{2}e^{-j\varphi_1}/2 & 0 & 0 & 0 \\ \sqrt{2}e^{-j\varphi_2}/2 & 0 & 0 & 0 \end{bmatrix} \tag{2}$$

where φ_1 , φ_2 , φ_3 are the phase shift of the S-parameters. To the BTSE power divider in this paper, φ_1 , φ_2 , φ_3 are set to $\varphi_1=\pi/2$, $\varphi_2=-\pi/2$, $\varphi_3=\pi$ .So we can get the mixed-mode S-matrix:

$$[S_M]=\begin{bmatrix} 0 & 0 & -\frac{\sqrt{2}}{2}j & \frac{\sqrt{2}}{2}j \\ 0 & -1 & 0 & 0 \\ -\frac{\sqrt{2}}{2}j & 0 & 0 & 0 \\ \frac{\sqrt{2}}{2}j & 0 & 0 & 0 \end{bmatrix} \tag{3}$$

In order to get the traditional S-matrix to derive the key design parameters, we need to know the transformation between mixed-mode S-matrix and traditional S-matrix. To simplify the calculation, we rearrange the traditional S-matrix: Supposing a network containing N balanced ports and M single ports, the traditional S-matrix is rearranged as this block matrix:

$$[S]=\begin{bmatrix} [S_{aa}]_{M\times M} & [S_{ab}]_{M\times N} & [S_{ac}]_{M\times N} \\ [S_{ba}]_{N\times M} & [S_{bb}]_{N\times N} & [S_{bc}]_{N\times N} \\ [S_{ca}]_{N\times M} & [S_{cb}]_{N\times N} & [S_{cc}]_{N\times N} \end{bmatrix} \tag{4}$$

where a,b,c respectively represents the single-ended port, the positive end of the balanced port and the negative end of the balanced port.

Based on these and derivation of the relationship between mixed-mode S-matrix and traditional S-matrix in [12], we can get:

$$[S]=\frac{1}{2}\times\begin{bmatrix} 2S_{SS} & \sqrt{2}(S_{SD}+S_{SC}) & \sqrt{2}(-S_{SD}+S_{SC}) \\ \sqrt{2}(S_{DS}+S_{CS}) & S_{DD}+S_{CD}+S_{DC}+S_{CC} & -S_{DD}-S_{CD}+S_{DC}+S_{CC} \\ \sqrt{2}(-S_{DS}+S_{CS}) & -S_{DD}+S_{CD}-S_{DC}+S_{CC} & S_{DD}-S_{CD}-S_{DC}+S_{CC} \end{bmatrix} \tag{5}$$

So we can get the traditional S-matrix to the BTSE power divider in this paper:

$$[S]=\begin{bmatrix} S_{22} & S_{23} & S_{1+2} & S_{1+3} \\ S_{32} & S_{33} & S_{1-2} & S_{1-3} \\ S_{21+} & S_{21-} & S_{1+1+} & S_{1+1-} \\ S_{31+} & S_{31-} & S_{1-1+} & S_{1-1-} \end{bmatrix}=\begin{bmatrix} 0 & 0 & -\frac{1}{2}j & \frac{1}{2}j \\ 0 & 0 & \frac{1}{2}j & -\frac{1}{2}j \\ -\frac{1}{2}j & \frac{1}{2}j & -\frac{1}{2} & -\frac{1}{2} \\ \frac{1}{2}j & -\frac{1}{2}j & -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{6}$$

According to the constraint conditions, the four-port S-parameters of the BTSE power divider are derived. The BTSE power divider can be built up with the structure shown in Fig.2:

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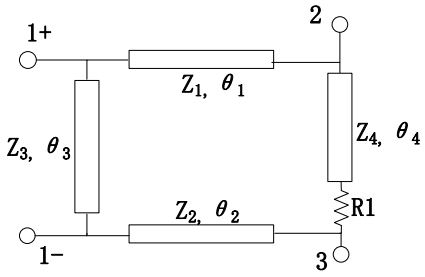

Fig. 2. Structure of the BTSE power divider

As shown in Fig.2, this BTSE Wilkinson power divider consists of four transmission lines and a resistance with the electrical lengths of the transmission lines are $\theta_1 = \theta_2 = \pi/2$ and $\theta_3 = \theta_4 = \pi$. While Z1, Z2, Z3, Z4 and R1 are to be determined. All the four ports have the same port impedance of $Z_0 = 50\Omega$.

In order to determine the critical parameters, the structure is analyzed by simplifying it to two-port network with other ports matched at the central frequency. As shown in Fig.3,

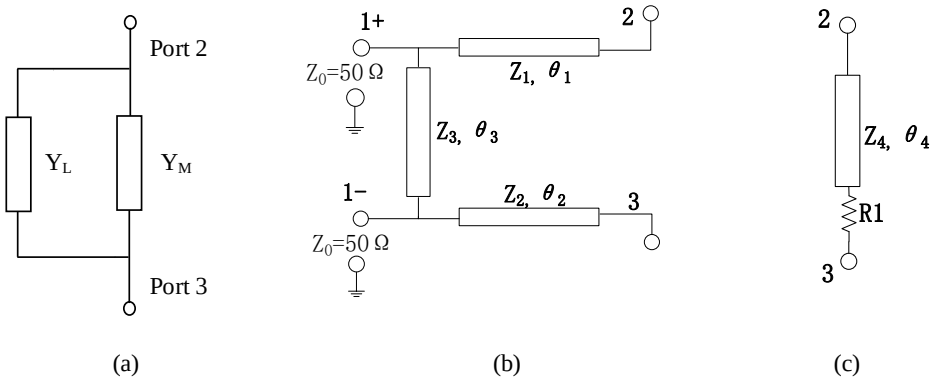

Fig. 3. Network between 2 and 3:(a) The equivalent network between port 2 and 3;(b) The circuit represented by Y_L;(c) The circuit represented by Y_M

using (6) we get:

$$[S]_{23} = \begin{bmatrix} S_{22} & S_{23} \\ S_{32} & S_{33} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{7}$$

According to (7) and the relationship between S-matrix and admittance matrix, we have:

$$[Y]_{23} = \begin{bmatrix} Y_0 & 0 \\ 0 & Y_0 \end{bmatrix} \tag{8}$$

where $Y_0 = 1/50\Omega^{-1}$ is the admittance of each port. The admittance matrix of the network can also be expressed as:

$$[Y]_{23} = [Y]_L + [Y]_M \tag{9}$$

Based on Fig.3 (b) and (c) we can get theirs ABCD matrix:

$$[ABCD]_L = \begin{bmatrix} 0 & jZ_1 \\ jY_1 & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_0 & 1 \end{bmatrix} \begin{bmatrix} 0 & jZ_2 \\ jY_2 & 0 \end{bmatrix} = \begin{bmatrix} \frac{Z_1}{Z_2} & 2Z_1Z_2Y_0 \\ 0 & \frac{Z_2}{Z_1} \end{bmatrix} \tag{10a}$$

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$$[ABCD]_M = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} 1 & R_1 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} -1 & -R_1 \\ 0 & -1 \end{bmatrix} \tag{10b}$$

According to (10) and the relationship between ABCD-matrix and admittance matrix, we get:

$$[Y]_L = \begin{bmatrix} \frac{1}{2Z_1^2 Y_0} & -\frac{1}{2Z_1 Z_2 Y_0} \\ -\frac{1}{2Z_1 Z_2 Y_0} & \frac{1}{2Z_2^2 Y_0} \end{bmatrix} \tag{11a}$$

$$[Y]_M = \begin{bmatrix} \frac{1}{R_1} & \frac{1}{R_1} \\ \frac{1}{R_1} & \frac{1}{R_1} \end{bmatrix} \tag{11b}$$

Based on the comparison of (8), (9) and (11), we have:

$$\begin{cases} \frac{1}{2Z_1^2 Y_0} + \frac{1}{R_1} = \frac{1}{2Z_2^2 Y_0} + \frac{1}{R_1} = Y_0 \\ -\frac{1}{2Z_1 Z_2 Y_0} + \frac{1}{R_1} = 0 \end{cases} \tag{12}$$

The solution of this equation system is $Z_1 = Z_2 = Z_0$ and $R_1 = 2Z_0$ where $Z_0 = 1/Y_0$.

From the above results, we can know that Z_3 and Z_4 can be freely selected. In this paper, we set $Z_3 = Z_4 = Z_x$ at central frequency. Next, the impact of the freely selected variable Zx on the relative bandwidth (BW) of the power divider will be introduced.

From the above discussion, we can know that the parameters in the matrix blocks S_{SS}, S_{CS}, S_{DD} (isolation, common-mode rejection, and differential-mode return loss) mainly determine the performance of the power divider. We define the minimum relative bandwidth of these parameters as the relative bandwidth of the power divider. Fig.4 presents the Zx in the range of (20Ω< ZX <200Ω), with the relative bandwidth with the trend of Zx change. It can be seen when the Zx is equal to 60Ω, the power divider get the maximum relative bandwidth of 27.5%. We take $Z_x = 50\Omega$ as an example to realize and test the proposed power divider.

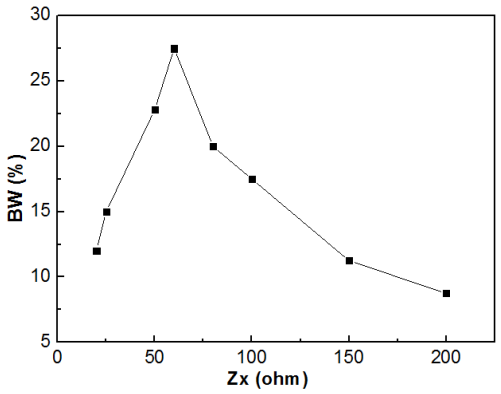

Fig. 4. Relationship Between Z_x and the relative bandwidth

III. REALIZATION OF BTSE POWER DIVIDER

According to the above analysis and design, a balanced-to-single-ended power divider is realized, as shown in Fig.5. It is fabricated on a 0.508-mm-thick Rogers4003 substrate, with $\varepsilon_r = 3.55$ and

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$\tan\delta = 0.0027$. The operating band is centered at $f_0 = 2.4GHz$. The positive and negative terminals of the balanced input port 1 are located on the left, while the two single-ended outputs are on the right. The geometric parameters in Fig.5 are L=12 mm, L1=18.5 mm, L2=37 mm, L3=12 mm, W1=1.13 mm, W2=1.13 mm, W3=1.13 mm, g=1.2 mm.

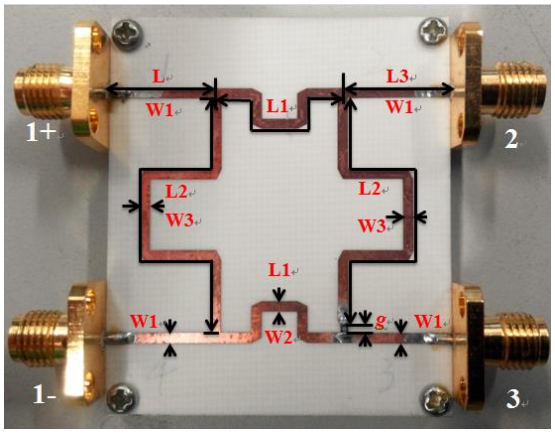
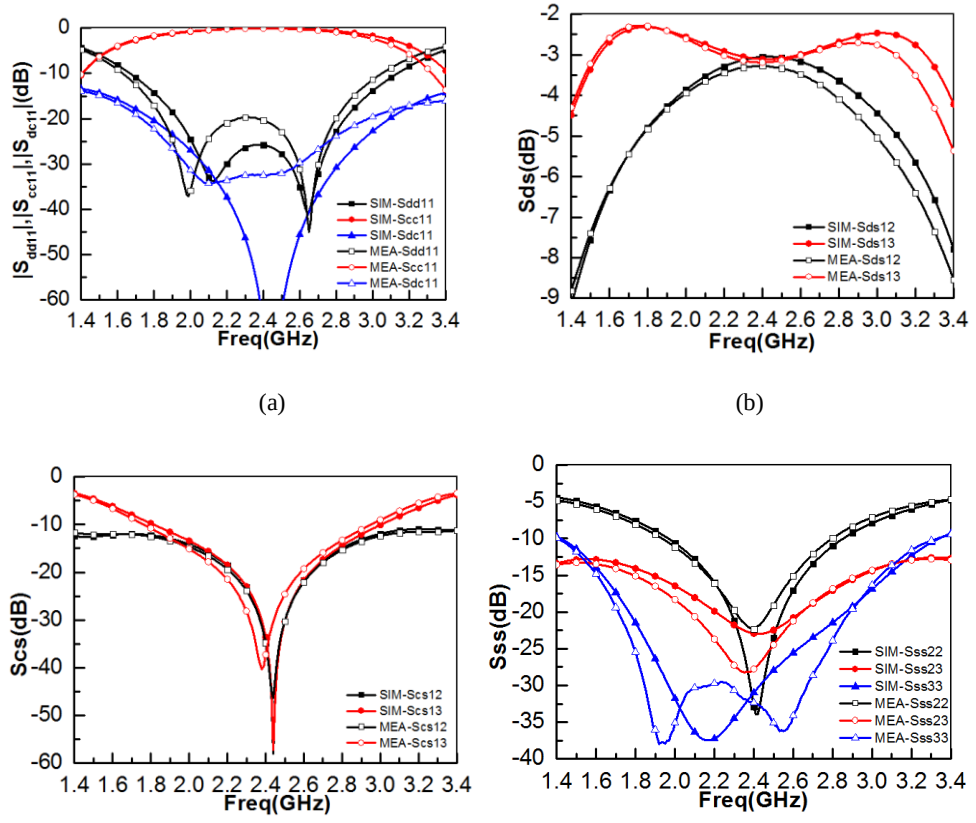


Fig. 5. Photo of the BTSE power divider

Finally, the simulated results and measured results obtained by Ansoft HFSS and Aglient E5071 are all shown in Fig.6.



(a) (b)

(c) (d)

Fig. 6. Simulated and measured results of the BTSE power divider prototype:(a) Parameters of balanced port 1;(b) Differential mode transmission parameters S_{ds};(c) Common mode transmission parameters $|S_{cs}|$;(d) Return loss and isolation of ports 2 and 3.

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As we can see, good performances have been successfully achieved with the proposed BTSE power divider. At center frequency 2.4GHz, the measured differential-mode transmissions are: |Sds12|=-3.25dB, |Sds13|=-3.17 dB; common-mode transmission parameters |Scs12|, |Scs13| are respectively -30.5dB and -28.6dB; differential-mode return loss of port 1 is |Sdd11|=-25.1 dB while common-mode return loss is |Scc11|=-0.10dB; the return loss of ports 2 and 3 are |Sss22|=-22.3dB, |Sss33|=-32.4dB; isolation parameters between 2 and 3(|Sss23|)is -23.7dB. The common-mode transmissions, the differential-mode return loss, the return loss of ports 2 and 3, the isolation between 2 and 3 are all lower than -15dB between 2.16 GHz~2.61 GHz. The relative bandwidth is 20%. Due to the error of the device fabrication and parameter testing, the experimental results and the simulated results have some differences in some parameters (Sdc11 and Sss33). Except this, the simulated results and the experimental results are in good agreement.

IV. CONCLUSION

Balanced-to-single-ended power divider makes up for the lack of performance when connect balanced devices and single-ended devices in many systems, and the research of this power divider is particularly important. A BTSE Wilkinson power divider of planar microstrip structure is proposed, investigated, and fabricated in this paper based on the theory of mixed-mode S parameters and the admittance matrix method. At center frequency 2.4GHz, differential-mode transmissions are|Sds12|=-3.25dB, |Sds13|=-3.17 dB, common-mode transmissions|Scs12|, |Scs13|are respectively -30.5dB and -28.6dB, common-mode return loss|Scc11|is -0.10dB, differential-mode return loss is|Sdd11|=-25.1 dB, isolation|Sss23|is -23.7dB. The 15dB relative bandwidth is about 20%. The simulated and measured results show its great merits of low insertion loss, good return loss, high isolation and high common-mode rejection (common-mode transmissions). Therefore, power divider designed in this paper can meet the requirements of most radar and communication systems.

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