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Closed-loop Implementation of a Non-isolated High Step-up Integrated SEPIC-CUK DC-DC Converter Structure with Single Switch

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HIGHLIGHTS

- The proposed converter topology employs single control switch.
- Improved voltage gain is obtained due to hybridization of SEPIC and CUK topologies.
- The input current is continuous during all modes of converter operation.
- The dynamic performance of the converter is improved with FOPID controller.

Abstract: Recently, the renewable energy applications require the development of highly efficient DC-DC converters with higher voltage transfer gain capability to meet out the increased global power demand. The non-isolated DC-DC converters are preferred due to certain drawbacks of isolated structures. The traditional boost, SEPIC (single-ended primary-inductor converter), and CUK based DC-DC converter structures are modified with additional power switches, diodes, and passive components in order to achieve high voltage gain. However, the modified structures with large number of active and passive elements suffer from the drawbacks of increased complexity of control algorithm, reduced power conversion efficiency and higher converter cost. Hence, the researchers started to explore more on single power switch configured non-isolated high step-up DC-DC converter topologies using hybrid concept. The research work presented in this paper explores such a high gain single-switch hybrid DC-DC converter structure that combines the conventional SEPIC and CUK topologies to achieve enhanced voltage gain. In the proposed hybrid topology, the input current is continuous during all modes of converter operation. Moreover, the power switch experiences only low voltage-current stress. The closed-loop configuration of the proposed hybrid converter is implemented using classic PID (Proportional+Integral+Derivative) and FOPID (Fractional Order PID) controllers, and simulated in MATLAB / SIMULINK environment with duty ratio D = 0.7 for the power switch. The results demonstrate that the dynamic performance of the converter with FOPID controller is much improved in terms of reduced settling time, overshoot, and ripples for the output voltage, as compared to that with classic PID controller.

Keywords: closed-loop configuration; CUK converter; duty ratio; FOPID controller; hybrid DC-DC converter topology; MATLAB / SIMULINK; PID controller; SEPIC topology; voltage gain.

INTRODUCTION

Over recent decades, renewable energy system based electrical energy generation is widely employed to meet out the rapidly growing energy demand worldwide as the non-renewable fossil fuels such as coal, natural gas, and petroleum are rapidly depleting and contribute mainly to the global warming, immense environment pollution, and increased cost of the system [1], [2]. The renewable energy sources like photo-voltaic (PV) panels and fuel cells (FC) deliver the electrical power at low DC output voltage level [3], [4]. High step-up DC-DC converters are employed to increase this low output voltage to high DC voltage level that can be fed as input to the grid-connected inverters [5]-[10]. The performance of renewable energy system based power generation thus depends mainly on the appropriate selection of highly efficient and cost-effective DC-DC converters capable of achieving high voltage gain.

The categories of high step-up DC-DC converters include transformer-based (isolated) and transformerless (non-isolated) structures. The transformer-based DC-DC converter topologies, suitable for high power applications, employ high-frequency transformers to provide electrical barrier between input and output ports of the converter. This electrical barrier helps to provide protection of the sensitive loads [11]. Another advantage of galvanically isolated DC-DC converter topologies is that they are capable to provide high voltage gain suitable for electric vehicles and renewable energy applications [12]-[16]. The important demerits of such isolated topologies are that the control switches are subjected to high frequency voltage transients due to isolation transformer's leakage inductance; two-stage power conversion process such as DC-AC-DC is involved; and complexity of control circuitry is increased. Hence, the non-isolated DC-DC converter configurations find more applications in electric vehicles and renewable energy system based power generation [17]-[18].

A non-isolated highly efficient hybrid topology of single-switch configured boost and Cuk converters is presented in [19]. The proposed lower component-count configuration under continuous current mode operation in [19] has high voltage gain capability than that of traditional boost and Cuk converters. A non-isolated integrated boost and modified Cuk converters with enhanced voltage gain is presented in [20]. The steady state behavior and state space modeling of the hybrid topology are better explained in [20]. The hybrid converter configuration proposed in [20] can provide higher voltage gain than that of the configuration proposed in [19].

A SEPIC converter capable of producing a stable and controlled output voltage using PID controller tuned by Bat Algorithm optimization method is proposed in [21]. The proposed PID controlled SEPIC converter in [21] has better dynamic performance in the presence of load and line disturbances. A combined SEPIC-Boost converter using several PID feedback tuning methods suitable for renewable energy applications is presented in [22]. The authors of [22] concluded that an extremely well-regulated output voltage is obtained using SEPIC-Boost converter with modified Ziegler-Nichols tuned PID controller. The performances of a linear PID controller and a nonlinear fuzzy controller are compared in terms of output voltage regulation in the presence of input voltage disturbances for a SEPIC converter proposed in [23]. A closed loop implementation with optimized FOPID controller for a conventional SEPIC topology can give the better voltage regulation [24].

A Cuk converter can well regulate the output voltage using PI/PID and fuzzy controllers [25, 26]. An application of Cuk converter for charging a lithium polymer battery of 12 V and 40 AH rating is presented in [27], where the converter output voltage is stabilized by PI control. A high performance PID controller, that can ensure a stabilized DC output voltage in the presence of small and large signal disturbances, is designed based on internal model control (IMC) principle for a reduced-order model of the Cuk converter proposed by the authors in [28]. A PI control based voltage tracking of bridgeless power factor correction (BPFC) Cuk converter is proposed in [29], which has the advantages of faster steady state response and lower output voltage ripples. The output voltage of an Interleaved Cuk Converter (ICC) can be regulated using Genetic Algorithm (GA) tuned FOPID controller in the presence of input voltage variations [30]. The stabilization of output voltage of linearized model of a non-isolated DC-DC Cuk converter can be exercised in the presence of any disturbance, using GA tuned FOPID controller as suggested by the authors in [31]. Some authors suggested a Cuk converter with well-regulated output voltage using PSO (Particle Swarm Optimization) tuned FOPID controller [32].

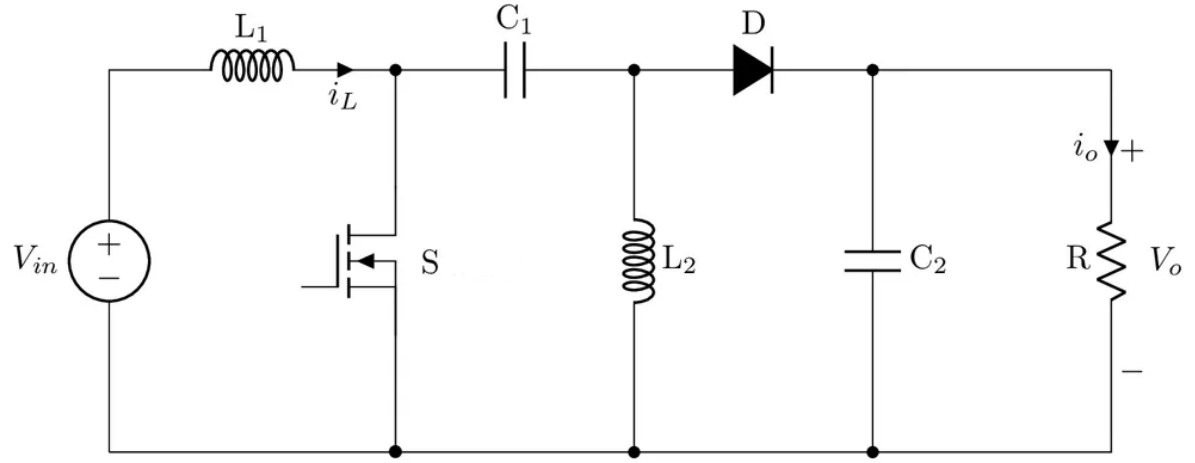
In this work, a hybridized non-isolated single-switch DC-DC converter topology with high voltage gain suitable for renewable energy applications is suggested. The traditional SEPIC and Cuk topologies are connected in parallel to obtain the proposed hybrid topology operating in continuous conduction mode. The active and passive components experience low voltage stress. This hybrid structure produces the enhanced voltage gain by complementing the benefits of SEPIC and Cuk configurations. The voltages appearing across the two shunt capacitors at the load side are summed up to get the output voltage (V_0) in

the proposed converter topology. The closed-loop implementation of the proposed integrated structure with suitably tuned FOPID controller ensures the output voltage stabilization. The voltage conversion ratio of the proposed integrated structure is found to be greater than that of the classical SEPIC and Cuk topologies.

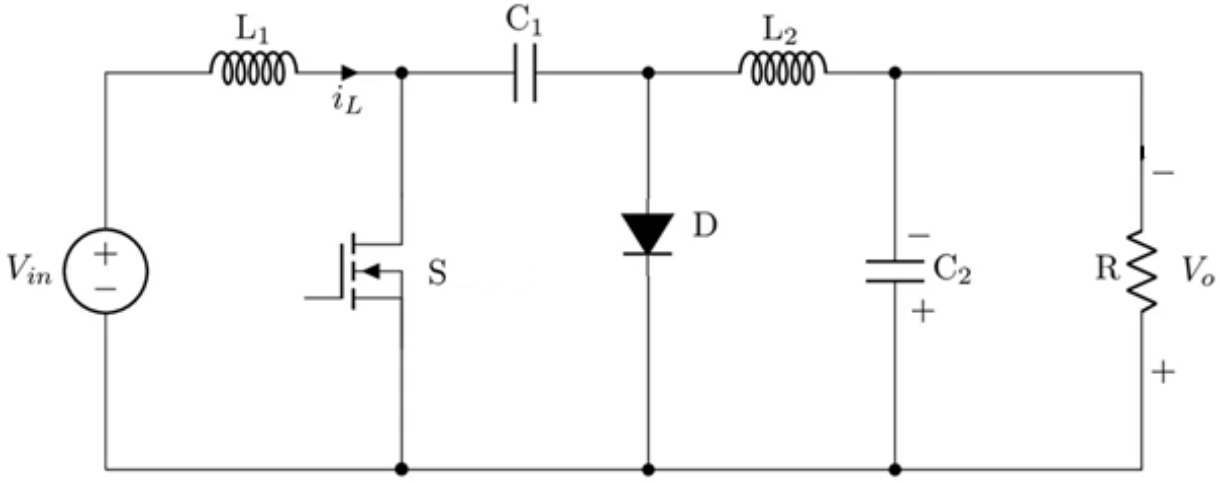
The structure of the remaining part of the paper is as follows: The various modes of operation, the derivation of static voltage gain, the simulation results and discussion of the proposed hybrid converter are presented in detail in subsequent sections that follow. The proposed converter has been simulated in MATLAB / SIMULINK platform and the corresponding results and discussion are presented in Section 3. The features of the proposed work are summarized in Conclusion section.

WORKING OF THE PROPOSED HYBRID CONVERTER STRUCTURE

The structures of traditional non-isolated DC-DC SEPIC and the CUK converter are depicted in Figure 1(a) and 1(b). Figure 1(c) shows the suggested non-isolated hybrid DC-DC converter topology with single control switch developed by parallel integration of the classical topologies shown in Figure 1(a) and 1(b) with common elements on the input side as control switch (S) and the inductor (L_1). The summation of the voltages appearing across the capacitors C_3 and C_4 is taken as load voltage (V_0). The integrated structure with ideal active and passive elements provides enhanced voltage gain than that of the conventional configurations shown in Figure 1(a) and Figure 1(b). The SEPIC converter can produce positive output and the CUK converter can produce negative output. However, the positive aspects of the proposed integrated converter are that (i). The integrated topology can produce positive (non-inverted) output, (ii). The voltage conversion ratio of the proposed integrated structure is found to be greater than that of the classical SEPIC and CUK topologies, (iii). Continuous currents are obtained at the input and output of the converter, and (iv). Low ripple current at both input and output of the converter. Moreover, the active and passive elements of the structure experience low voltage stress. There are three continuous conduction modes of operation of the proposed integrated converter structure.



(a)



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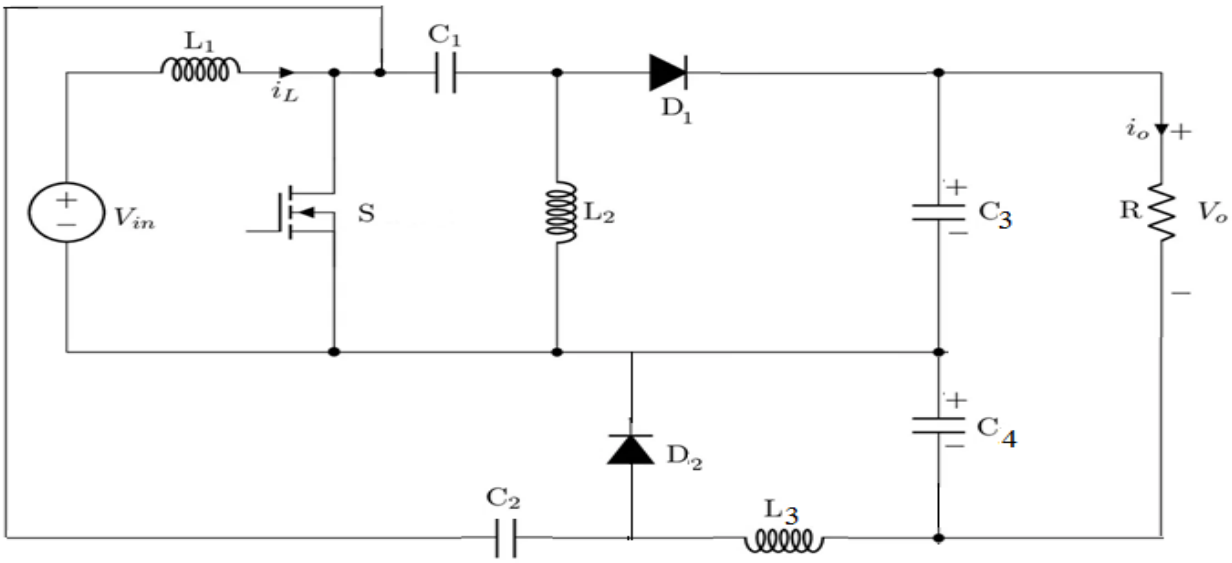

(c)

Figure 1. Topologies of DC-DC converter - **(a)**. Conventional SEPIC converter, **(b)**. CUK converter, **(c).** Proposed integrated converter.

Operation of the converter during Mode-I ($t_0<t<t_1$):

During Mode-I operation, the power switch S is in ON condition. The diodes D_1 and D_2 are open circuited due to reverse bias. The inductor L_1 is charged to supply voltage V_{in}. The capacitor C_1 charges the inductor L_2. The inductor L_3 is magnetized by the capacitors C_2 and C_4. The load voltage V_0 is obtained by the discharge of the capacitor C_3. The equivalent circuit for Mode-I is shown in Figure 2(a). The voltages across the inductors L_1, L_2, and L_3 are shown by the following Equation (1).

$$V_{L1} = V_{in}; \qquad V_{L2} = V_{C1}; \qquad V_{L3} = V_{C2} - V_{C4} \tag{1}$$

where, V_{L1}, V_{L2}, & V_{L3} are the voltages across the inductors L_1, L_2, & L_3 respectively;
V_{in} is DC input voltage;
V_{C1}, V_{C2}, & V_{C4} represent respectively the voltages across the capacitors C_1, C_2, & C_4.

Operation of the converter during Mode-II ($t_1<t<t_2$):

During Mode-II operation, the power switch S is in OFF condition. The diode D_1 is open circuited due to reverse bias and the diode D_2 acts as short circuit due to forward bias condition. The inductor L_1 gets demagnetized and hence charges the capacitor C_2 through the forward biased diode D_2. There is no demagnetization path for the inductor L_2 due to reverse biased diode D_1 and OFF condition of the switch S. Hence, there is no current flow through the inductor L_2. The inductor L_3 discharges its stored energy through the forward biased diode D_2 and hence charges the capacitor C_4. The capacitor C_3 supplies the load current (I_0). The corresponding equivalent circuit for Mode-II is shown in Figure 2(b). The following Equation (2) illustrates the inductors' voltages.

$$V_{L1} = V_{in} - V_{C2}; \qquad V_{L2} = 0; \qquad V_{L3} = -V_{C4} \tag{2}$$

Operation of the converter during Mode-III ($t_2<t<t_3$):

During Mode-III operation, the power switch S remains in the OFF condition. Both the diodes D_1 and D_2 start conducting. The inductor L_1 charges the capacitor C_2. The inductor L_2 charges the capacitor C_3 through the forward biased diode D_1. The inductor L_3 charges the capacitor C_4 through the forward biased diode D_2. The source V_{in} supplies the load R_0. The corresponding equivalent circuit for Mode-III is shown in Figure 2(c). The following Equation (3) illustrates the inductors' voltages.

$$V_{L1} = V_{in} - V_{C2}; \qquad V_{L2} = -V_{C3}; \qquad V_{L3} = -V_{C4} \tag{3}$$

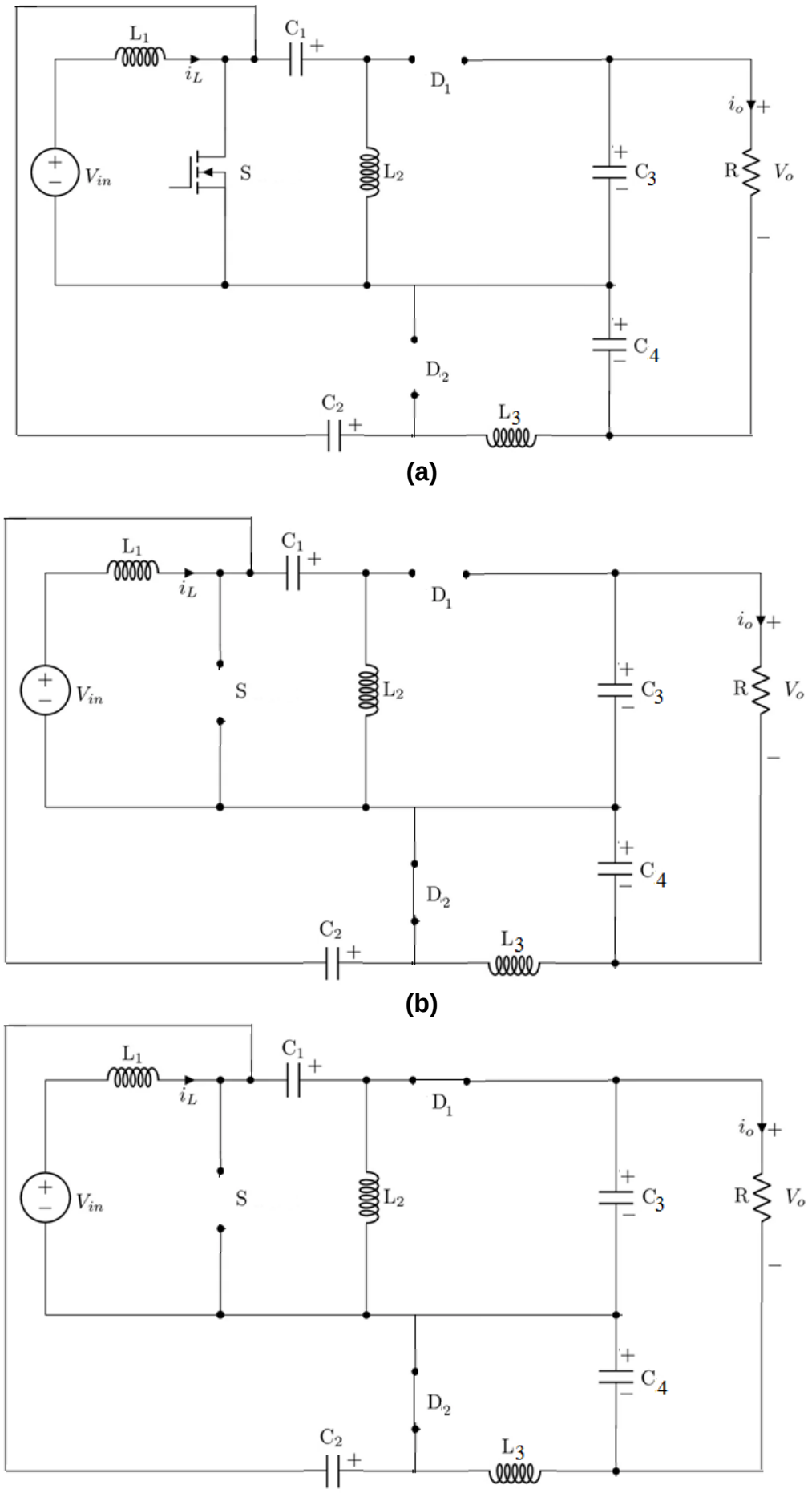

Figure 2. Equivalent circuits of the suggested DC-DC converter - (a). Mode-I (b). Mode-II (c). Mode-III

Derivation of voltage gain of the proposed converter:

For the traditional continuous conduction mode (CCM) operated SEPIC and Cuk converter configurations, with duty ratio 'k' for the power switch, shown in Figure 1(a) and 1(b), the voltage gain equations (4) & (5) are illustrated as shown below:

$$\text{Voltage gain } (G_{CCM}) \text{ for the traditional SEPIC topology} = \frac{V_0}{V_{in}} = \frac{k}{1-k} \tag{4}$$

$$\text{Voltage gain } (G_{CCM}) \text{ for the traditional Cuk converter} = \frac{V_0}{V_{in}} = -\frac{k}{1-k} \tag{5}$$

The Equations (1), (2), & (3) are used to derive the voltage gain equation for the proposed integrated SEPIC-Cuk DC-DC converter topology based on the volt-second balance principle applied to the three inductors L_1, L_2, and L_3.

$$V_{in}kT_s + (V_{in} - V_{C2})(1-k)T_s = 0 \tag{6}$$

$$V_{in}kT_s - V_{C3}(1-k)T_s = 0 \tag{7}$$

$$(V_{C2} + V_{C4})kT_s - V_{C4}(1-k)T_s = 0 \tag{8}$$

From the Equation (6), the voltage V_{C2} across the capacitor C_2 is obtained as Equation (9).

$$V_{C2} = \frac{V_{in}}{1-k} \tag{9}$$

From the Equations (7) & (8), the voltages V_{C3} & V_{C4} across the capacitors C_3 & C_4 are obtained.

$$V_{C3} = V_{C4} = \frac{kV_{in}}{(1-k)} \tag{10}$$

The load voltage (V_0) of the proposed converter is obtained as the sum of the capacitor voltages V_{C3} and V_{C4}.

$$V_0 = V_{C3} + V_{C4} = \frac{2k}{(1-k)} V_{in} \tag{11}$$

The voltage gain (G_{CCM}) of the proposed integrated SEPIC-Cuk DC-DC converter is obtained as:

$$G_{CCM} = \frac{V_0}{V_{in}} = \frac{2k}{1-k} \tag{12}$$

CONTROLLERS FOR THE PROPOSED INTEGRATED CONVERTER STRUCTURE

Suitable controllers are employed to obtain the stabilized output from the converter in the presence of any disturbances. In this work, classical PID (Proportional+Integral+Derivative) controller and FOPID (Fractional Order PID) controllers are used.

Classical PID controller:

The general form of classical PID controller is PID. The transfer function of the controller is given by Equation (13). In this work, the PID controller parameters such as K_p, K_i, & K_d are tuned by trial and error approach. Accordingly, suitable parameters are chosen and are shown in Table 2.

$$C(s) = \frac{Y(s)}{E(s)} = K_p + \frac{K_i}{s} + K_d s \tag{13}$$

Fractional Order PID (FOPID) controller:

The general form of Fractional Order PID (FOPID) controller is $PI^{\lambda}D^{\mu}$. The transfer function of the controller is given by Equation (14). The FOPID controller constants such as K_p, K_i, K_d, λ, and μ are also selected based on trial and error approach and are tabulated in Table 3.

$$C(s) = \frac{Y(s)}{E(s)} = K_p + \frac{K_i}{s^{\lambda}} + K_d s^{\mu} \tag{14}$$

where, λ is integral order; μ is differential order. By suitable selection of these two parameters, the FOPID controller is made to have better control effect [33, 34].

DESIGN OF THE PROPOSED INTEGRATED CONVERTER CIRCUIT COMPONENTS

The power switch 'S', and the diodes D_1 and D_2 are assumed to be ideal semiconductor devices. The inductors (L_1, L_2, and L_3) and capacitors (C_1, C_2, C_3, and C_4) of the proposed converter are designed so that the power switch 'S' has to support for both the converter voltage and current.

Design of inductors and capacitors:

The proposed converter has an input voltage (V_{in}) of 24 V and output voltage (V_0) of 112 V supplying a 85 W load. The duty ratio (k) of the power switch is selected as 0.7. Hence, the output voltage of SEPIC converter portion (V_{So}) and the Cuk converter portion (V_{Co}) in the integrated structure is 56 V each. The switching frequency (f_s) is 15 kHz. The values of all inductors and capacitors used in the proposed converter are so designed that the change in inductor and capacitor currents) is no more than 4%, the output ripple voltage is no more than 1%, and the ripple voltage across the capacitors is no more than 5% [35].

$$L_1 \geq \frac{V_{in}^2 V_{So}}{f_s (V_{in} + V_{So}) P_o (\%\Delta I_{L1}^{min})} \geq \frac{(24)^2 \times 56}{15000 \times (24+56) \times 85 \times 4} \geq 79\,\mu H$$

The value of L_1 is taken as 100 μH for optimum performance of the converter.

$$L_2 \geq \frac{2V_{in} V_{So}^2}{f_s (V_{in} + V_{So}) P_o (\%\Delta I_{L2}^{max})} \geq \frac{2 \times 24 \times (56)^2}{15000 \times (24+56) \times 85 \times 3} \geq 492\,\mu H$$

$$L_3 \geq \frac{2V_{in} V_{So}^2}{f_s (V_{in} + V_{So}) P_o (\%\Delta I_{L3}^{max})} \geq \frac{2 \times 24 \times (56)^2}{15000 \times (24+56) \times 85 \times 3} \geq 492\,\mu H$$

The values of L_2 and L_3 are taken as 700 μH each for optimum performance of the converter.

$$C_1 \geq \frac{P_0}{f_s \times 2(V_{in} + V_{So})^2 (\%\Delta V_{C1}^{max})} \geq \frac{85}{15000 \times 2 \times (24+56)^2 \times 3} \geq 0.15\,\mu F$$

$$C_2 \geq \frac{P_0}{f_s \times 2(V_{in} + V_{So})^2 (\%\Delta V_{C2}^{max})} \geq \frac{85}{15000 \times 2 \times (24+56)^2 \times 3} \geq 0.15\,\mu F$$

The values of C_1 and C_2 are taken as 3.3 μF each for optimum performance of the converter.

$$C_3 \geq \frac{P_0}{f_s \times 2(V_{in} + V_{So}) V_{So} (\%\Delta I_{C3}^{max})} \geq \frac{85}{15000 \times 2 \times (24+56) \times 56 \times 3} \geq 0.211\,\mu F$$

$$C_4 \geq \frac{P_0}{f_s \times 16 V_{Co}^2 (\%\Delta V_{C4}^{max})} \geq \frac{85}{15000 \times 16 \times (56)^2 \times 1} \geq 0.113\,\mu F$$

The values of C_3 and C_4 are taken as 0.5 μF each for optimum performance of the converter.

SIMULATION OF THE PROPOSED INTEGRATED CONVERTER: RESULTS AND DISCUSSION

The simulation models of the suggested integrated DC-DC converter configuration with PID and FOPID controllers are developed using MATLAB/SIMULINK software tool as shown in Figure 3 and Figure 4. The variable-step solver of type 'ode 45' is used for simulating the converter at 15 kHz switching frequency (f_s). Table 1, Table 2, and Table 3 respectively list the values of converter circuit parameters, PID controller parameters, and FOPID controller parameters used for simulation. A PWM (Pulse Width Modulation) pulse as shown in Figure 5 is generated using pulse generator for triggering the MOSFET switch S into conduction. The duty cycle 'k' for the power switch S is considered to be varying from 0.5 to 0.9. A resistive load of 150 Ω resistance with 85 W power capacity is used. In this work, the simulation results are shown for k = 0.7. A DC source (V_{in}) of 24 V, as shown in Figure 6, is given as input voltage to the proposed converter. Figure 7 shows the waveform of DC input current (I_{in}) with 3.874 A as steady state value. Figure 8 and Figure 9 show the DC output voltage (V_0) and DC output current (I_0) waveforms of the converter with PID and FOPID controllers, which indicate that the converter with FOPID controller performs better than that with classical PID controller in terms of reduced overshoot and reduced settling time. The three inductors' voltages V_{L1}, V_{L2}, & V_{L3} are illustrated in Figure 10, Figure 11, and Figure 12 respectively for the converter with FOPID controller. The waveforms of voltages V_{C1}, V_{C2}, V_{C3}, & V_{C4} across the four capacitors C_1, C_2, C_3, & C_4 are respectively shown in Figure 13, Figure 14, Figure 15, and Figure 16 for the converter with FOPID controller. The sum of voltages V_{C3} & V_{C4} gives the output voltage (V_0) of the converter. Figure 17 and Figure 18 illustrate that the voltage stress across the diodes D_1 and D_2 is found to be low. The voltage stress and current stress of the power switch are indicated by the waveforms shown in Figure 19 and Figure 20 for the converter with PID and FOPID controllers. It is understood that the power switch is subjected to low voltage and current stress for the case of converter with FOPID controller. For k = 0.7, the proposed converter has the efficiency (η_c) of 90% as calculated below:

$$\eta_c = \frac{P_0}{P_{in}} \times 100 = \frac{V_0 I_0}{V_{in} I_{in}} \times 100 = \frac{112 \times 0.7474}{24 \times 3.874} \times 100 = 90\%$$

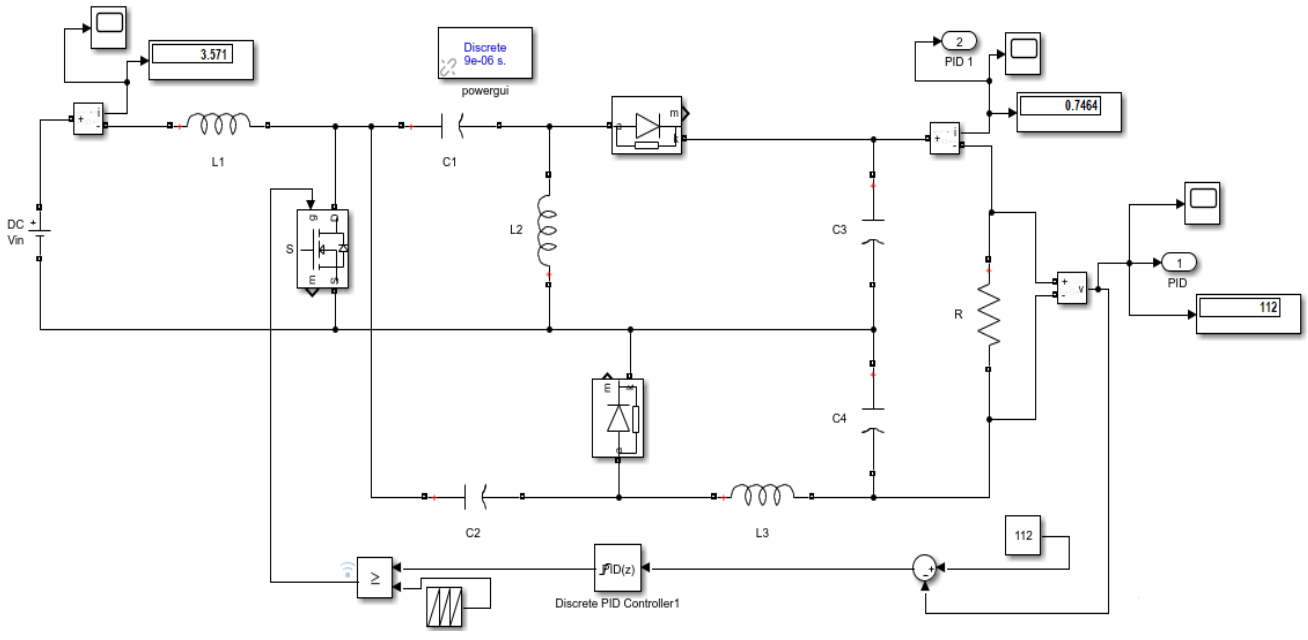

Figure 3. MATLAB / SIMULINK model of the proposed integrated DC-DC converter with PID controller

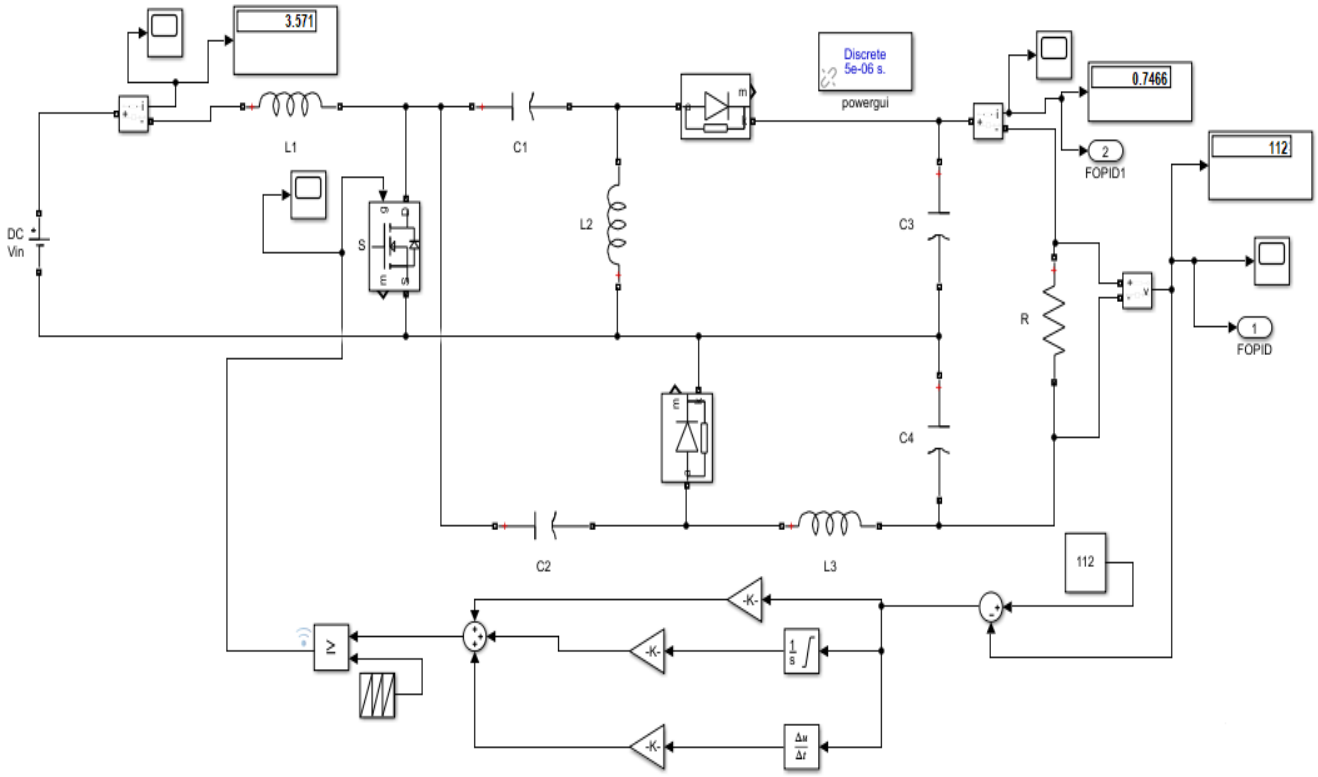

Figure 4. MATLAB / SIMULINK model of the proposed integrated DC-DC converter with FOPID controller

Table 1. Parameters used for the simulation of the proposed hybrid DC-DC converter

Parameters	Symbol	Value
Input voltage	V_{in}	24 V (DC)
Output voltage	V_0	112 V (DC)
Inductor	L_1	100 µH
Inductors	L_2, L_3	700 µH each
Capacitors	C_1, C_2	3.3 µF each
Capacitors	C_3, C_4	0.5 µF each
Switching frequency	f_s	15 kHz
Load resistance	R_0	150 Ω
Load power	P_0	85 W
Average output current	I_0	0.7474 A
Duty ratio of the switch	D	0.7

Table 2. PID controller parameters

Parameters	Symbol	Value
Proportional gain	K_p	5.6×10^{-5}
Integral gain	K_I	2
Derivative gain	K_d	1×10^{-5}

Table 3. FOPID controller Parameters

Parameters	Symbol	Value
Proportional gain	K_p	3.47×10^{-3}
Integral gain	K_I	1
Derivative gain	K_d	1×10^{-5}
Differential order	µ	4.568×10^{-4}
Integral order	λ	0.37

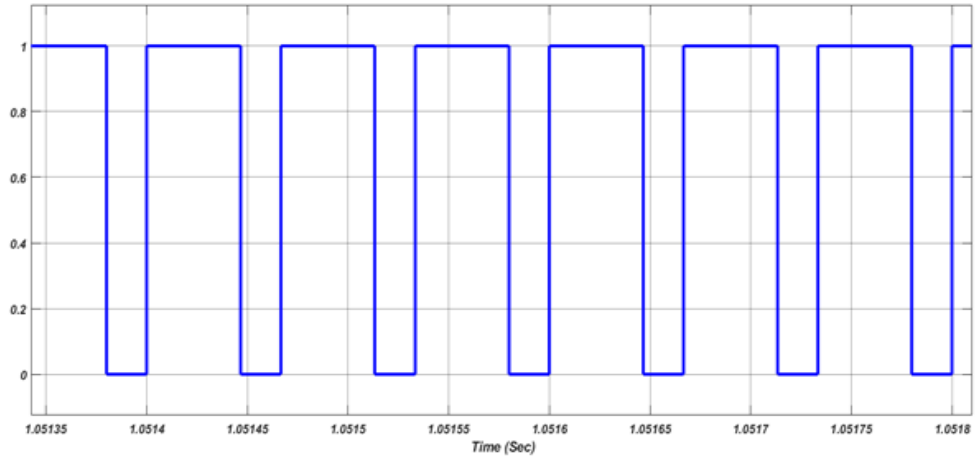

Figure 5. Gate pulse waveform for the switch S

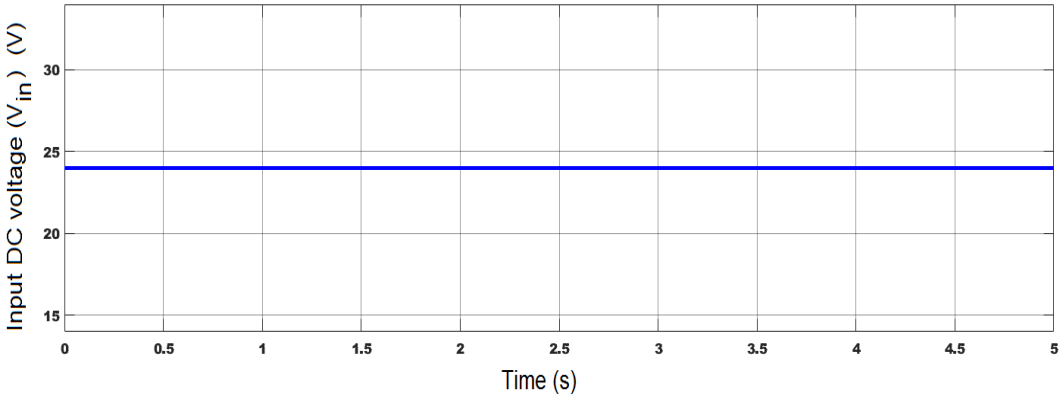

Figure 6. Input DC voltage (V_{in})

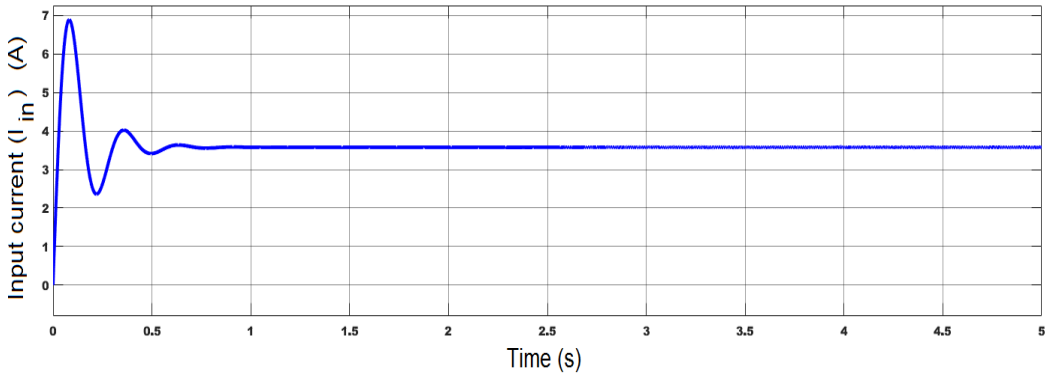

Figure 7. Input DC current (I_{in})

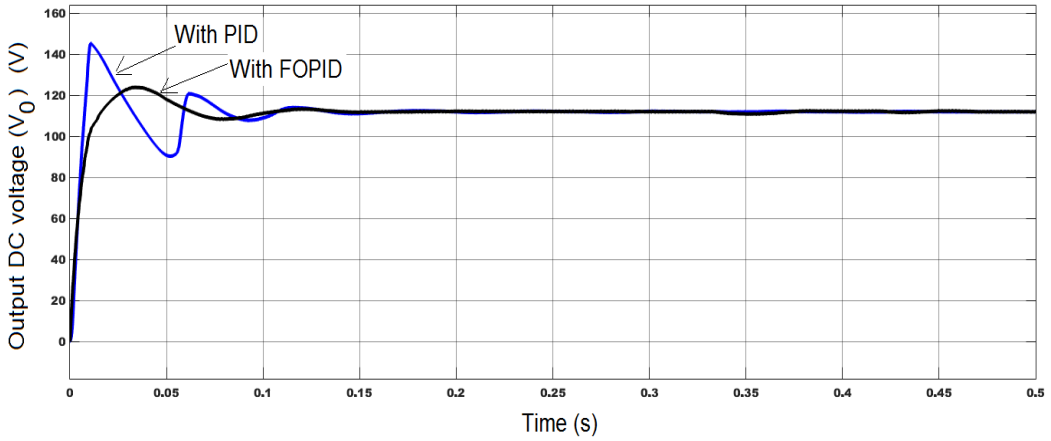

Figure 8. Output DC voltage (V_0) with PID and FOPID controllers

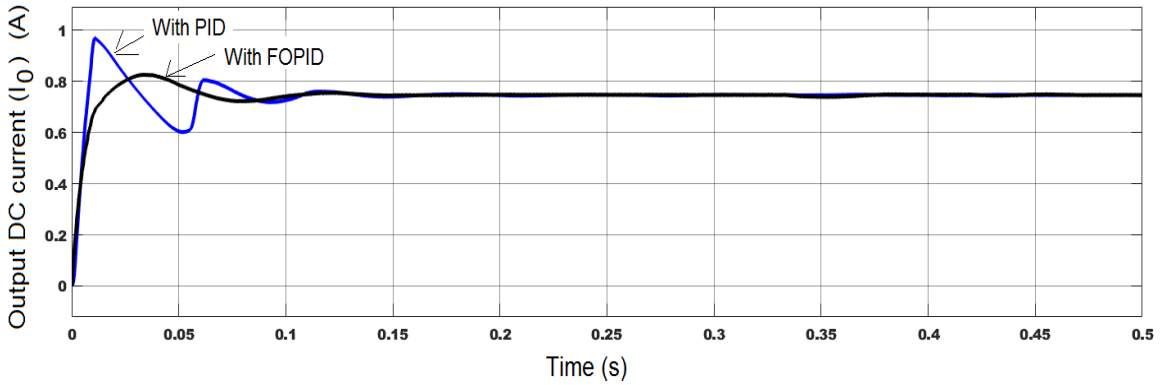

Figure 9. Output DC current (I_0) with PID and FOPID controllers

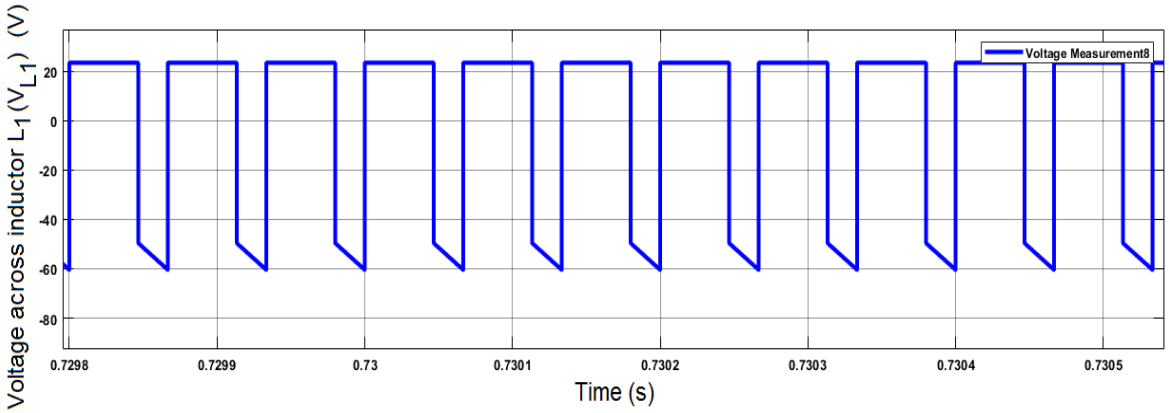

Figure 10. Voltage across inductor L_1 (V_{L1})

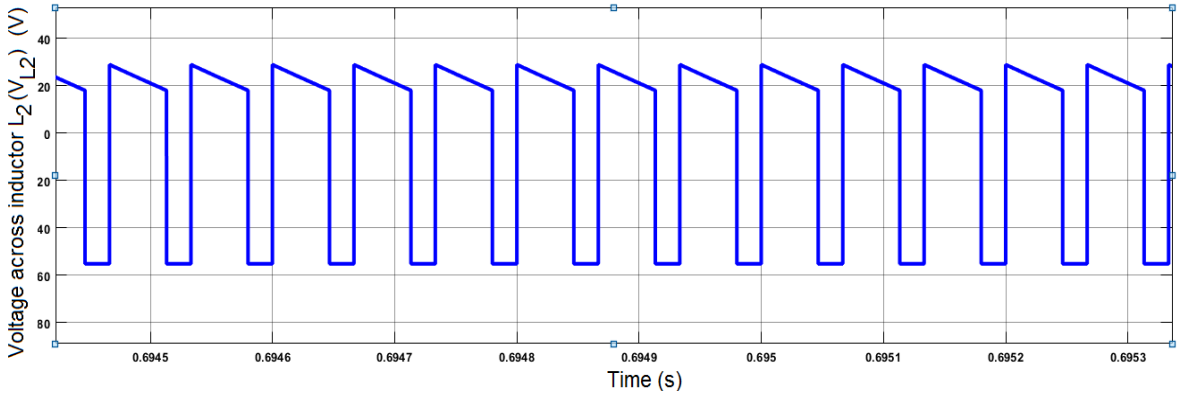

Figure 11. Voltage across inductor L_2 (V_{L2})

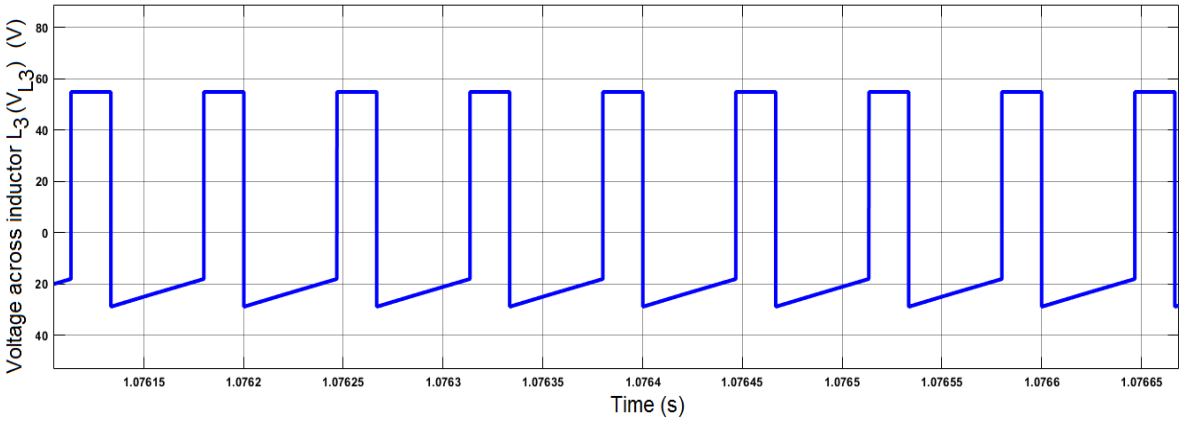

Figure 12. Voltage across inductor L_3 (V_{L3})

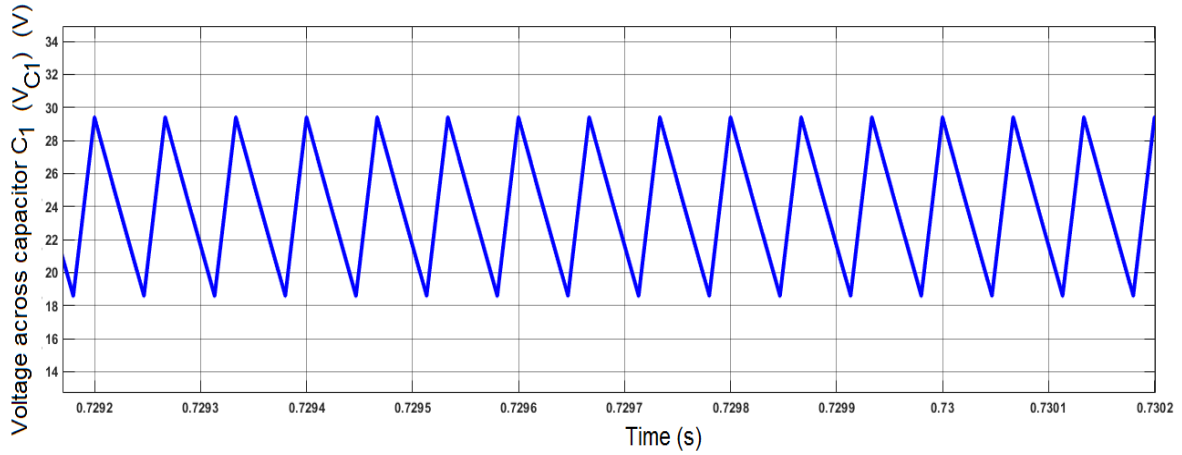

Figure 13. Voltage across capacitor C_1 (V_{C1})

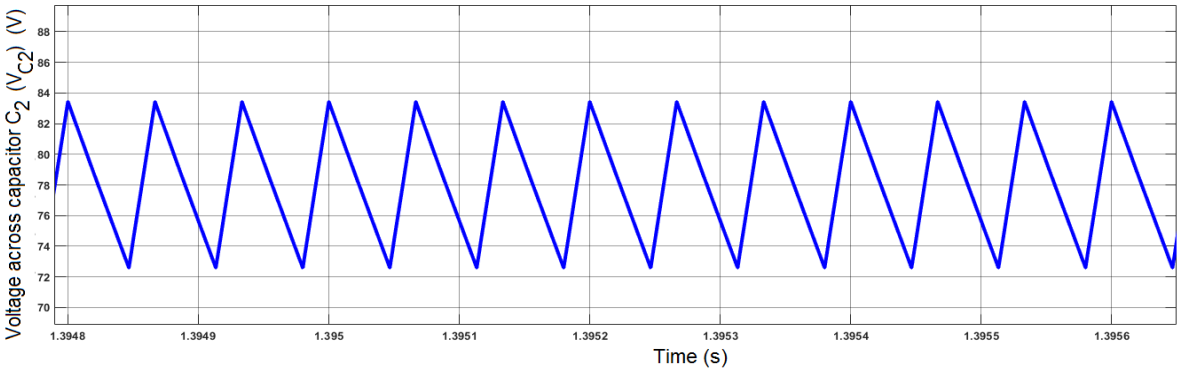

Figure 14. Voltage across capacitor C_2 (V_{C2})

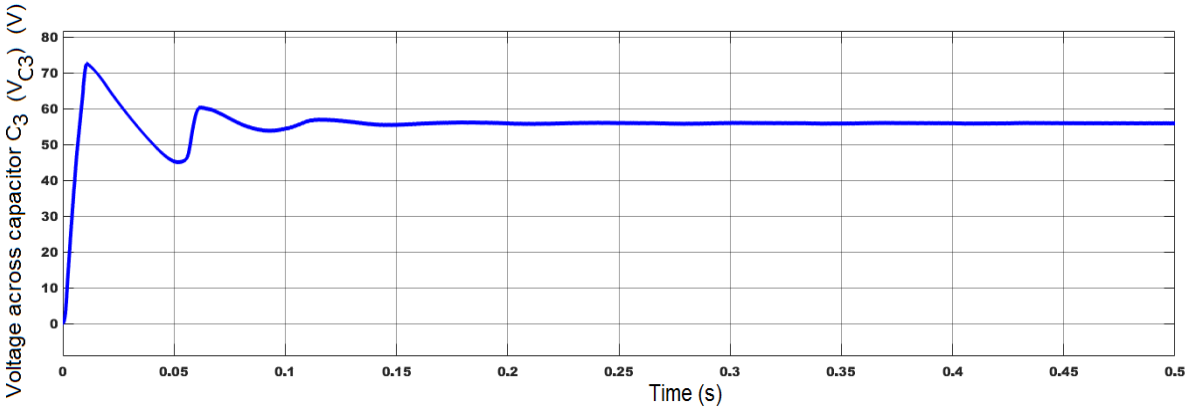

Figure 15. Voltage across capacitor C_3 (V_{C3})

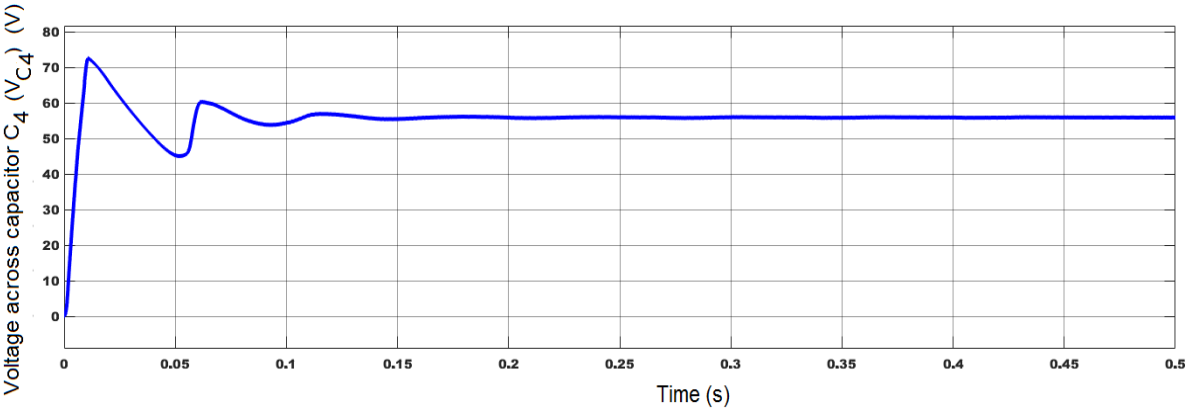

Figure 16. Voltage across capacitor C_4 (V_{C4})

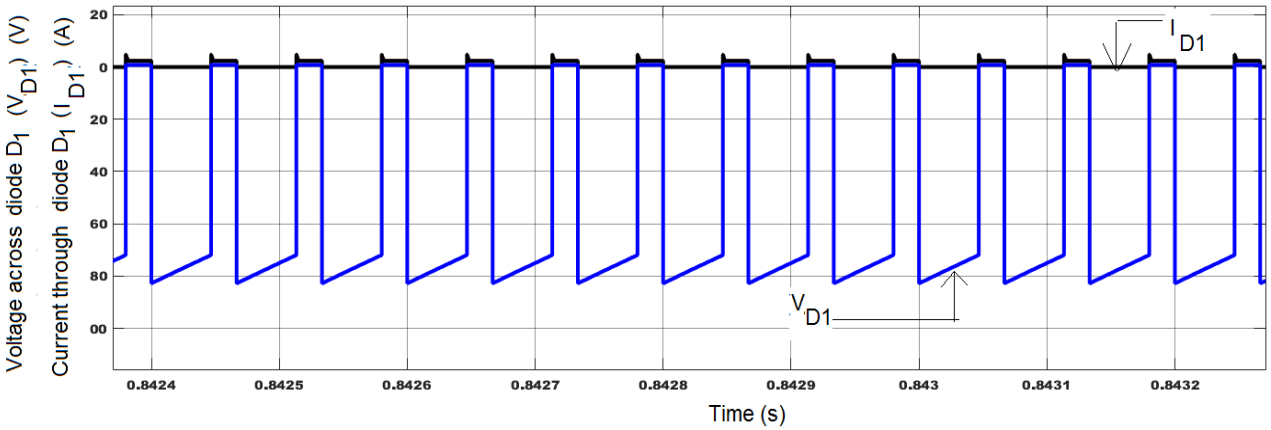

Figure 17. Voltage across diode D_1 (V_{D1}) and Current through diode D_1 (I_{D1})

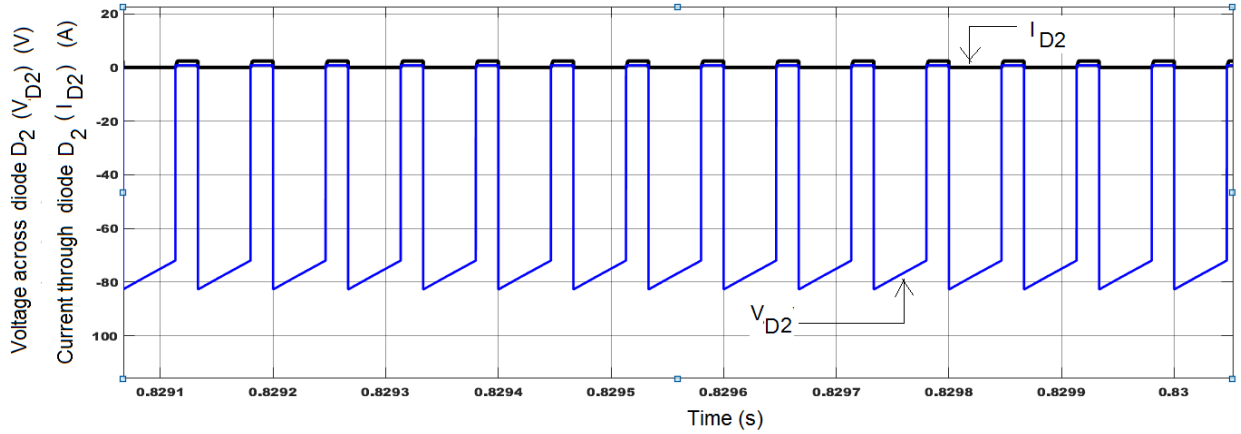

Figure 18. Voltage across diode D_2 (V_{D2}) and Current through diode D_2 (I_{D2})

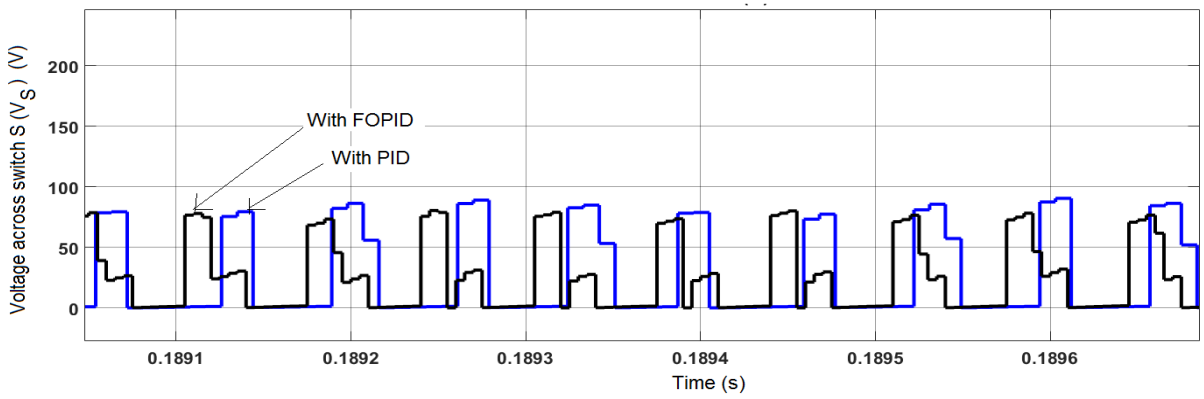

Figure 19. Voltage stress across switch S (V_S)

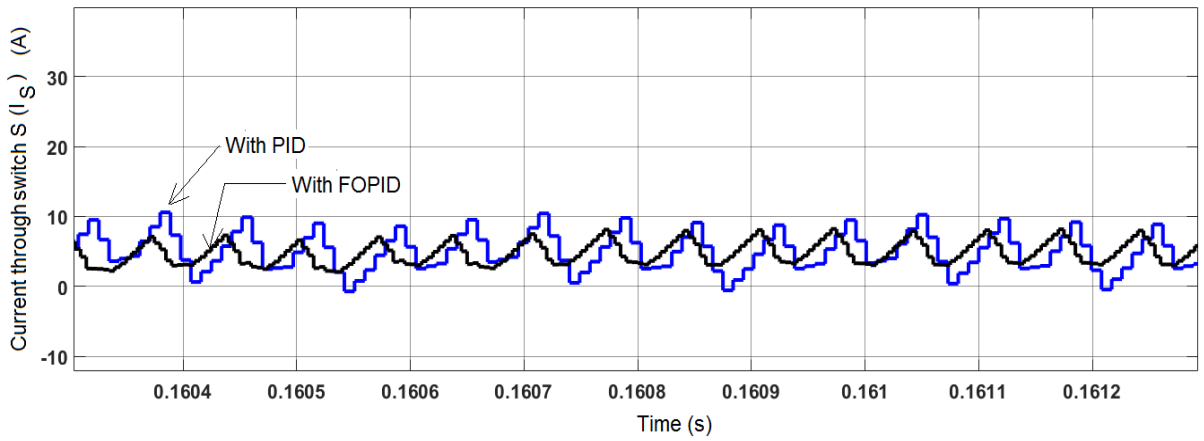

Figure 20. Current stress of switch S (I_S)

CONCLUSION

In this research article, the steady state performance of a non-isolated integrated single-switch SEPIC-Cuk DC-DC converter structure with PID and FOPID controllers has been analyzed. The suggested closed-loop configuration of the converter with positive output is operated in continuous inductor current mode. The integrated structure has high voltage gain compared to the traditional SEPIC / Cuk topologies. The performance validation of the proposed converter with duty ratio k = 0.7 is carried out using MATLAB / SIMULINK tool. The output voltage and output current waveforms of the converter are presented for the converter with suitably tuned PID and FOPID controllers. The reduced overshoot and reduced settling time are observed on both output voltage and output current waveforms for the case of converter with FOPID control scheme than that with PID controller. Thus, the FOPID controller improves the dynamic performance of the converter. The voltages across the inductors, capacitors, and the diodes of the converter with FOPID control are also presented for the same k = 0.7. The approximate power conversion efficiency of the proposed converter with k = 0.7 is calculated as 90%. Moreover, low voltage-current stress is observed on the power switch and the diodes for the case of converter with FOPID control scheme. The selection of output side capacitors C_3 and C_4 is in such a way that ripples are very much minimized in both the output voltage and current. The salient features of the proposed integrated DC-DC converter structure make it suitable for renewable energy based power generation applications.

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