Vol.67: e24240081, 2024
https://doi.org/10.1590/1678-4324-2024240081
ISSN 1678-4324 Online Edition

BABT
Brazilian Archives of Biology and Technology

Article - Engineering, Technology and Techniques

A 3-Phase Reduced Switch Count Symmetric 17-Level Inverter Topology Supplying a Resistive Load

Murali Duraisamy[1*]
https://orcid.org/0000-0002-6890-1687

[1]Government College of Engineering Srirangam, Tiruchirappalli, Department of Electrical and Electronics Engineering, Tamil Nadu, India.

Editor-in-Chief: Alexandre Rasi Aoki
Associate Editor: Daniel Navarro Gevers

Received: 25-Jan-2024; Accepted: 13-May-2024.

*Correspondence: muraliems@gmail.com; Tel.: +91-9894984592 (M.D.).

HIGHLIGHTS

- Reduced components are employed in the suggested inverter topology.
- Lower %THD is obtained with PDPWM strategy.
- COPWM method yields higher fundamental RMS and peak voltages at the inverter output.

Abstract: The work explored in this paper includes the simulation analysis pertaining to a 3-phase symmetric cascaded H-bridge configured multilevel inverter, capable of producing 17-levels of output voltages with lower number of switching devices, supplying a resistive load. The proposed inverter topology is implemented using Carrier Overlapping Pulse Width Modulation (COPWM), Variable Frequency PWM (VFPWM), and Phase Disposition PWM (PDPWM) techniques with sine wave reference. The losses due to switching and harmonic components in the output voltage are found to be low in the proposed multilevel inverter. The Matlab/Simulink platform is used to validate the performance of the inverter. The switching loss calculation, and the percentage value of THD (Total Harmonic Distortion) occurring in the inverter output voltage and currents are shown for the above mentioned PWM methods using modulation index parameters. The simulation results illustrate that the proposed inverter implemented with PDPWM methodology produces lower amount of harmonics in the inverter output voltage and current, and the inverter implemented with COPWM technique produces output voltages of higher RMS values of fundamental frequency.

Keywords: 17-level inverter; COPWM; Matlab/Simulink; PDPWM; Reduced switching devices; Switching loss; Total Harmonic Distortion; VFPWM.

INTRODUCTION

The power industries employ multilevel inverter topologies capable of producing high AC voltage and high power. The inverter's power rating can be enhanced by increasing the voltage levels without the need for higher current ratings on individual power device. The multilevel voltage source inverter structures without transformer or series connected synchronized power devices can produce high AC voltages with low harmonics content. There is a significant reduction in the amount of harmonics present in the inverter output voltage for increased levels of output voltage [1]. The multilevel functionality concept based inverters

are classified into three categories [2]. A cascaded H-bridge multilevel inverter structure employs lower component-count to obtain a particular number of levels of output voltage in comparison with that required for diode-clamped and flying-capacitor topologies. Multilevel functionality concept includes the features of improved power factor and enhanced power efficiency, and capable to produce lower voltage harmonic distortion on load side [3, 4]. However, the multilevel inverter structures suffer from the drawbacks such as complex control strategy, additional circuit components' requirement, increased inverter cost, and reduced reliability [4]. Therefore, the main concern in the design of multilevel structure is to reduce the number of components.

Reduced number of diodes and improved efficiency can be achieved using the nested multilevel converter structures [5]. A hybrid cascaded converter topology consisting of half-bridge cells to reduce losses and full-bridge cells to attenuate the harmonics is proposed in [6]. Furthermore, a hybrid converter can have scalability feature in case of high voltages. The simple control structure, low cost, and smaller space required for installation are the features of a reduced switch count cascaded inverter based on multilevel concept [7]. Another reduced switch configuration is proposed by some authors for multilevel DC link based 3-phase 7-level inverter topology [8]. A new reduced switch count multilevel inverter structure, in which inverter output voltage can be produced by combining DC input levels in additive and subtractive manner, was introduced by some authors. The proposed topology has low switching frequency operation with suitable modulation scheme [9]. A new group of symmetric and asymmetric multilevel inverter structures with reduced switch-count and minimized losses is presented in [10].

Some authors proposed the concept and features of single/3-phase versions of multilevel inverter with reduced power switches [11]. The structure proposed in [11] is capable of operating in both symmetrical and asymmetrical configurations and also to provide output voltage with lower harmonic contents. The harmonic analysis of a 3-phase 7-level inverter is presented in [12], where various carrier based sinusoidal modulation schemes such as phase opposition disposition PWM, phase disposition PWM, and alternate-phase opposition disposition are employed. A modified 3-phase inverter having lower number of components is proposed by some authors in [13]. The fundamental frequency control based topology proposed in [13] is capable to generate phase voltages with 7-levels and line voltages with 13-levels. This topology has simple architecture and control strategy [13]. A 3-phase 9-level cascaded trinary source inverter having simple architecture and control logic employs carrier based modulation techniques with trapezoidal reference [14].

This research article explores a 3-phase symmetric configured multilevel functionality concept based inverter powered by DC voltage sources that is capable of generating 17-levels of output voltages with lower switch-count. This article is organized to have five sections such as: (i). The concept of suggested 17-level inverter and switching loss calculation, (ii). The switching logic, (iii). A brief idea about various PWM techniques, (iv). The simulation analysis of the inverter and the results. This is followed finally by the conclusion part.

PROPOSED 17-LEVEL INVERTER TOPOLOGY

The suggested 3-phase cascaded symmetrical configured H-bridge inverter with 17-levels of output voltages, having eighteen power switches per phase, supplying a 3-phase resistive load of 60 Ω/phase connected in delta configuration, is shown in Figure 1. The proposed 3-phase inverter configuration has three numbers of single phase inverters energized by eight DC voltage sources, each of 80 V magnitude, per phase in isolated configuration to produce 17 numbers of output voltage levels. The positive and negative polarity of voltages can be produced by the inverter. The addition of modular stages can increase the inverter output voltage levels. Each power switch is a discrete IGBT (Insulated Gate Bipolar Transistor) with a monolithically integrated anti-parallel diode. The switches on the opposite legs of a phase are so connected that they will not conduct at the same instant. The voltage appearing across the pair of switches (S_1, S_1') and (S_9, S_9') is equal to V_{dc} for symmetrical input case, whereas for the remaining power switches, the voltage stress is $2V_{dc}$. For this inverter, always nine numbers of switches should conduct in various modes of operation. The output voltages due to three series-connected legs are added to obtain the voltage across the load. The suggested inverter has reduced number of power switches compared to that of traditional multilevel inverter and that of topology proposed in [15]. Table 1 shows the comparison of number of power switches employed in the suggested inverter with that of other topologies.

Table 1 Comparison of power switches of the proposed 17-level inverter with that of other topologies

Inverter category	No. of DC power supplies/phase	No. of power switches	No. of output voltage levels	No. of ON-state power switches
Traditional cascaded MLI [16]	k	4k	2k+1	2k
Cascaded MLI proposed in [17]	k	2k+4	2k+1	k+2
Proposed 17-level cascaded MLI	k	2k+2	2k+1	k+1

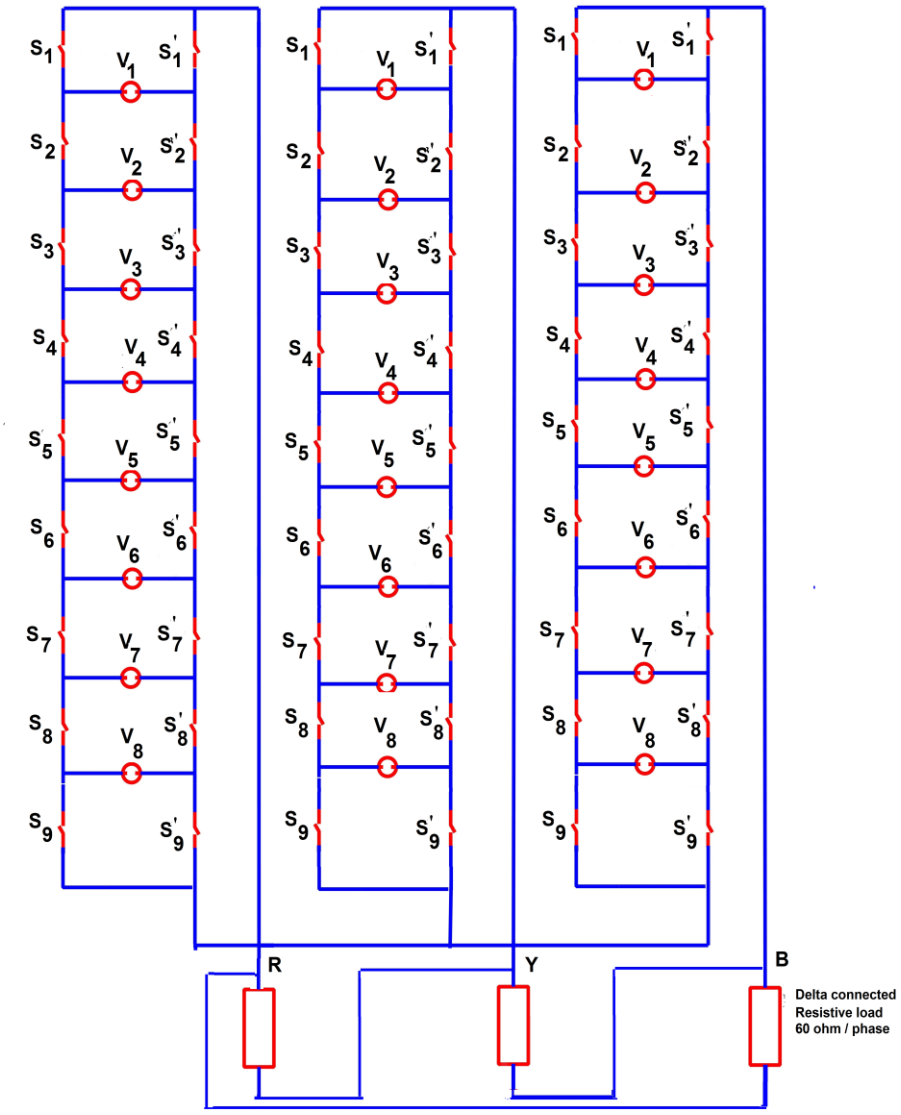

Figure 1. Proposed 3-phase 17-level inverter topology supplying a resistive load

In the proposed 17-level inverter, the switching losses occur during ON state and OFF state of the power IGBT switches. The total switching loss (P_{SW}) calculation of the proposed topology is based on the expression shown by Equation 1 [18-20].

$$P_{SW} = P_{SW,ON} + P_{SW,OFF} = \frac{1}{6} \times f_{SW} \times V_{SW} \times I(t_{ON} + t_{OFF}) \quad (1)$$

Where, $P_{SW,ON}$: switching power loss during ON state of the switch (W);

$P_{SW,OFF}$: switching power loss during OFF state of the switch (W);

f_{SW} : switching frequency (kHz); V_{SW} : peak voltage of the switch (V); I : current through the switch (A);

t_{ON} : time interval during which the switch is in ON state (ns);

$t_{ON} = t_{d-ON} + t_{r-ON}$; t_{d-ON} ; turn ON delay time (ns); t_{r-ON} : turn ON rise time (ns);

$t_{OFF} = t_{d-OFF} + t_{f-OFF}$; t_{d-OFF} : turn OFF delay time (ns); t_{f-OFF} : turn OFF fall time (ns);

For a typical IGBT, the following parameter values are taken:

$V_{SW} = 0.6$ V ; $t_{d-ON} = 100$ ns; $t_{r-ON} = 250$ ns; $t_{d-OFF} = 200$ ns; $t_{f-OFF} = 300$ ns.

The switching loss calculation for the power switches controlled by various PWM schemes discussed in the proposed work is given in Table 3.

SWITCHING LOGIC OF THE SUGGESTED 3-PHASE INVERTER TOPOLOGY

There are three single phase inverters used in the suggested 3-phase configuration of 17-level inverter, in which each phase contains eight isolated DC voltage sources (V_1 to V_8) and nine pair of power IGBT switches per phase such as (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), (S_4, S_4'), (S_5, S_5'), (S_6, S_6'), (S_7, S_7'), (S_8, S_8') and (S_9, S_9') respectively as shown in Figure 1. All eight DC voltage sources have magnitude of V_{dc} each. Table 2 shows the switching logic of different switches to obtain 17 levels of output voltages. These 17 levels of stepped output voltages are used to construct an approximate sinusoidal output AC voltage waveform. A particular output voltage level is obtained by turning ON of nine IGBT switches at a time.

Table 2. Switching logic for the proposed 17-level inverter structure

Levels	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_1'	S_2'	S_3'	S_4'	S_5'	S_6'	S_7'	S_8'	S_9'	Output voltages
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	$+8V_{dc}$
2	1	0	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1	1	$+7V_{dc}$
3	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1	0	0	0	$+6V_{dc}$
4	1	0	1	0	1	0	0	0	0	0	1	0	1	0	1	1	1	1	$+5V_{dc}$
5	1	0	1	0	1	1	1	1	1	0	1	0	1	0	0	0	0	0	$+4V_{dc}$
6	1	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	$+3V_{dc}$
7	1	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	$+2V_{dc}$
8	1	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	$+1V_{dc}$
9	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	$0V_{dc}$
10	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	$-1V_{dc}$
11	0	1	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	1	$-2V_{dc}$
12	0	1	0	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	$-3V_{dc}$
13	0	1	0	1	0	0	0	0	0	1	0	1	0	1	1	1	1	1	$-4V_{dc}$
14	0	1	0	1	0	0	1	1	1	1	0	1	0	1	1	0	0	0	$-5V_{dc}$
15	0	1	0	1	0	0	0	0	0	1	0	1	0	1	1	1	1	1	$-6V_{dc}$
16	0	1	0	1	0	0	0	1	1	1	0	1	0	1	1	1	0	0	$-7V_{dc}$
17	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	$-8V_{dc}$

SINUSOIDAL PWM SCHEMES FOR MULTILEVEL INVERTERS

There are three categories of PWM control strategies, such as Space vector PWM technique, fundamental switching frequency modulation method, and Carrier based modulation scheme, which find applications in various multilevel inverter topologies.

It is easier to implement the multicarrier PWM techniques to low voltage inverter modules. This technique uses the concept that the power devices can be switched ON by means of pulses obtained by the comparison of a carrier signal of triangular wave shape with sine wave reference. The %THD level in the output AC voltage is found to be low in this technique. In this research article, the multicarrier bipolar PWM methods such as Variable Frequency (VF), Carrier Overlapping (CO), and Phase Disposition (PD) PWM strategies are tried due to their merits over the other PWM techniques.

The Variable Frequency (VF) PWM method generates 17-level output by using 16 carrier signals of different frequencies and same amplitude. In variable frequency PWM method, all the power switches can be switched for equal number of times by increasing the frequency of carrier waves for the intermediate switches as shown in Figure 2. For intermediate power switches, the frequency ratio (m_f) is chosen as 70, and for the remaining power switches, the frequency ratio (m_f) and amplitude modulation index (m_a) and are chosen as 30 and 0.85 respectively.

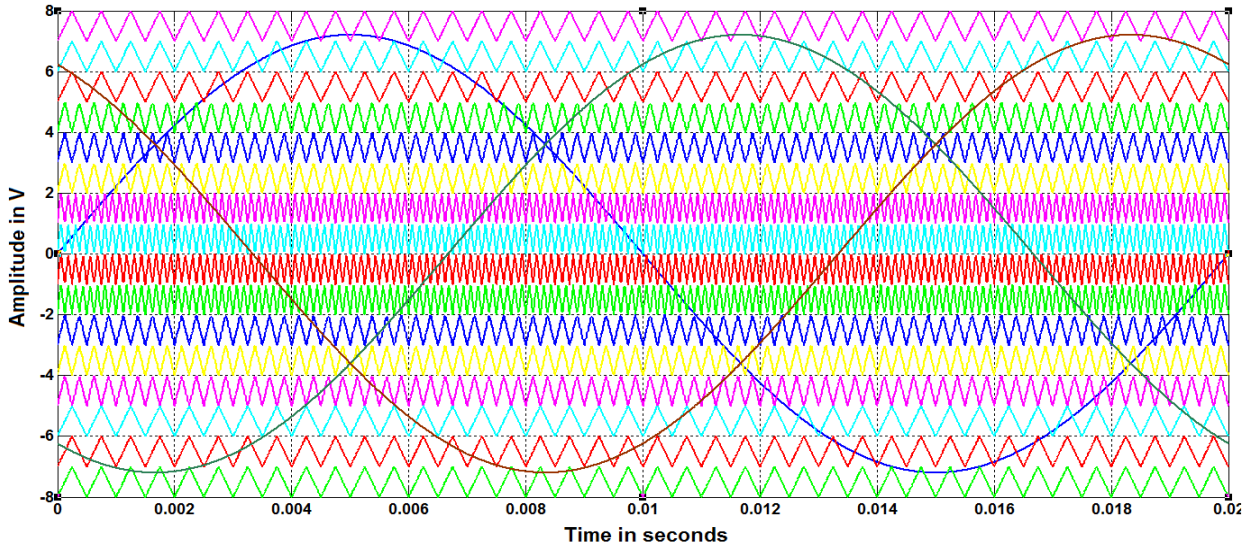

Figure 2. Carrier waveform and sine wave reference for VFPWM method

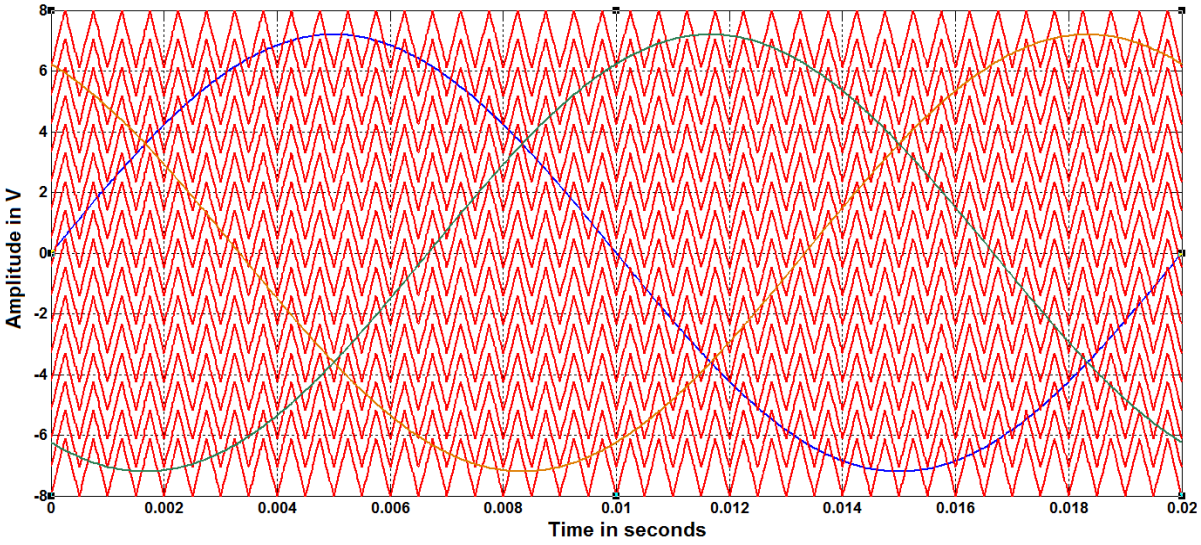

Figure 3. Carrier waveform and sine wave reference for COPWM method

The Carrier Overlapping PWM (COPWM) scheme necessitates (m-1) number of carrier signals of frequency f_c and peak-to-peak amplitude A_c for an m-level inverter. The multicarrier waveform and centrally located sine reference waveform of frequency f_s and amplitude A_s for COPWM method for amplitude modulation index m_a = 0.85 and frequency ratio m_f = 30 are shown in Figure 3. There is an overlapping of

bands that the (m-1) carriers occupy as shown in Figure 3. Each carrier wave has the overlapping vertical distance of (A_c/2). The amplitude modulation index m_a for COPWM strategy is given by Equation 2.

$$m_a = \frac{A_s}{0.25mA_c} \tag{2}$$

In the Phase Disposition PWM (PDPWM) strategy, there are several in-phase carrier signals with single sine modulation waveform as shown in Figure 4. The bands that all the in-phase carrier signals occupy are contiguous. The PDPWM method also requires (m-1) number of carrier signals of frequency f_c and peak-to-peak amplitude A_c for an m-level inverter. The sine reference waveform of frequency f_s and amplitude A_s placed at zero reference is compared continuously with the carrier waveforms. If the amplitude of sine wave reference exceeds that of a carrier wave, then the relevant switches are made to conduct. Otherwise, they will not be allowed to conduct. The sine wave is located centrally in the set of carrier waveforms. Equation 3 shows the definition of the amplitude modulation index (m_a) and frequency ratio (m_f) for PDPWM technique. In the simulation study, amplitude modulation index (m_a) and frequency ratio (m_f) are chosen as 0.85 and 30 respectively.

$$m_a = \frac{2A_s}{(m-1)A_c}; \quad m_f = \frac{f_c}{f_s} \tag{3}$$

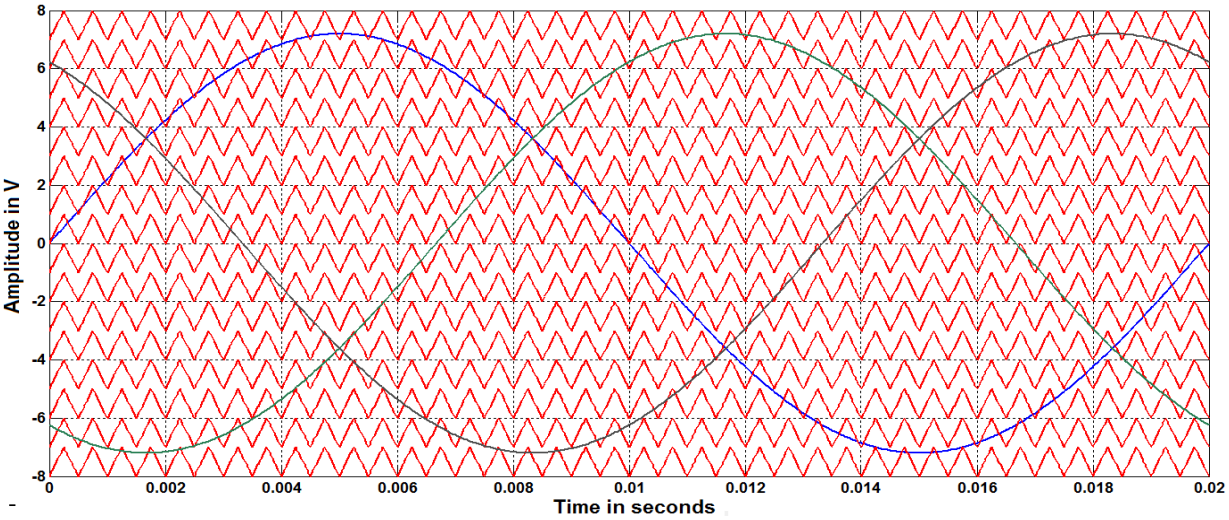

Figure 4. Carrier waveform and sine wave reference for PDPWM method

RESULTS AND DISCUSSION

The Matlab/Simulink software tool is used to simulate the suggested 3-phase 17-level inverter topology supplying a delta connected resistive load. For a delta connected load, the line and phase voltages are equal in magnitude. A filter inductor of inductance L_f = 4 mH/phase is used at the output of the proposed 17-level inverter, to reduce the harmonics present in the voltage and current waveforms [21]. The switching pulses are developed using various bipolar multicarrier sinusoidal PWM techniques such as VFPWM, COPWM, and PDPWM with 50 Hz (f_s) sinusoidal wave reference. The VFPWM strategy uses the frequency of triangular carrier wave as f_c = 2 kHz for modulation index m_f = 30, and f_c = 4 kHz for modulation index m_f = 70. The time domain simulations are carried out for m_a = 0.85 and 1 respectively. The simulation waveforms of the line voltages (= phase voltages), and the corresponding harmonic waveforms for the proposed 3-phase cascaded 17-level inverter with modulation index m_a = 0.85 are shown in Figure 5, Figure 11, Figure 17, Figure 6, Figure 12, and Figure 18 respectively. The FFT block is used to measure the % harmonic distortion (%THD). The RMS output voltage is found to be around 460 V with COPWM strategy, as shown in Figure 7. The lower %THD of voltage waveform is found to be 4.11% with PDPWM scheme as is evident from the Figure 18. The waveforms of line and phase currents, and the corresponding FFT spectra are illustrated in Figure 7, Figure 9, Figure 13, Figure 15, Figure 19, Figure 21, Figure 8, Figure 10, Figure 14, Figure 16, Figure 20, and Figure 22 respectively, for the three PWM schemes with m_a = 0.85. The lower %THD for phase and line currents is found to be 4.29 and 3.83 respectively, with PDPWM method as is clear by referring Figure 20 and Figure 22 respectively. Hence, the PDPWM scheme

is capable of producing lower %THD in both line voltage and current waveforms, and the COPWM strategy is responsible for producing higher RMS and peak values of line voltages Similarly, the performance factors of the proposed inverter are also calculated for amplitude modulation index value of $m_a = 1$.

The various performance factors of the proposed inverter topology are compared for PDPWM, VFPWM, and COPWM schemes with $m_a = 0.85$ and 1 respectively as shown by Table 3. The variation of switching loss and %THD for voltage and currents with switching frequency, under the three PWM schemes, is given in Table 4. Figure 23 and Figure 24 respectively illustrate the graphical variation of switching loss, and %THD of voltage and currents with switching frequencies. Hence, an appropriate switching frequency nearer to 6 kHz may be identified for the proposed inverter operation, as switching losses and %THD of voltage and currents are somewhat lower nearer to 6 kHz switching frequency.

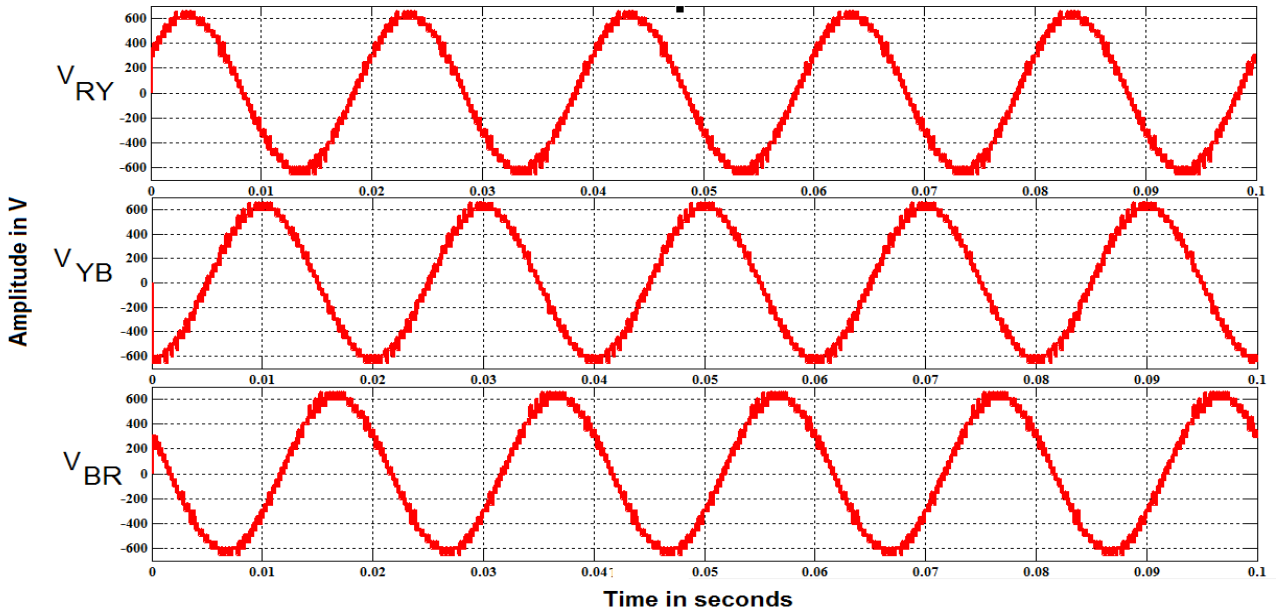

Figure 5. 3-phase line voltages generated by VFPWM strategy for the proposed inverter

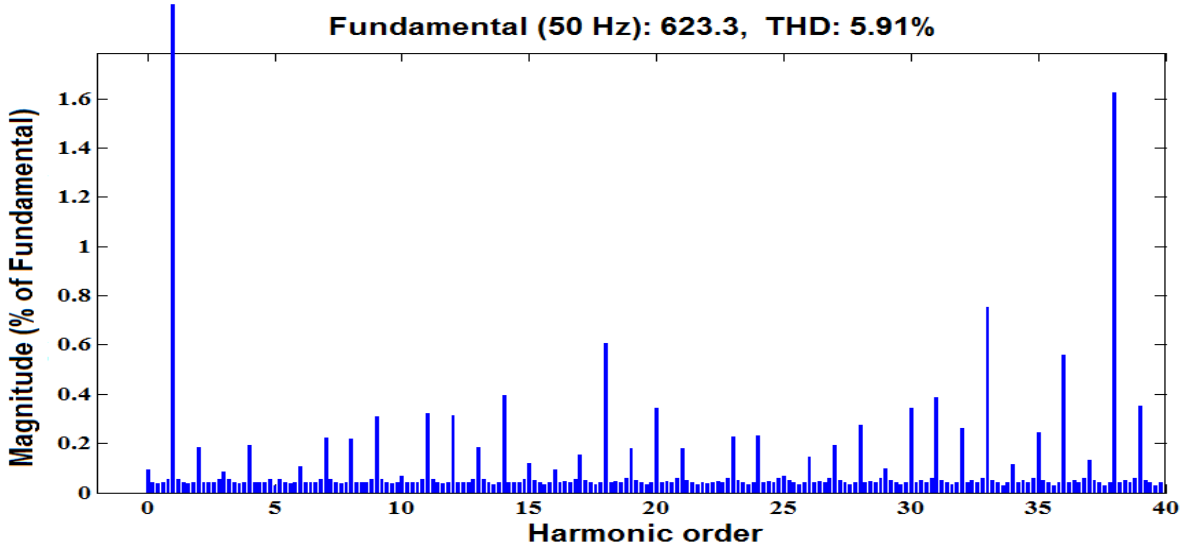

Figure 6. Harmonics present in 3-phase line voltages produced by VFPWM method

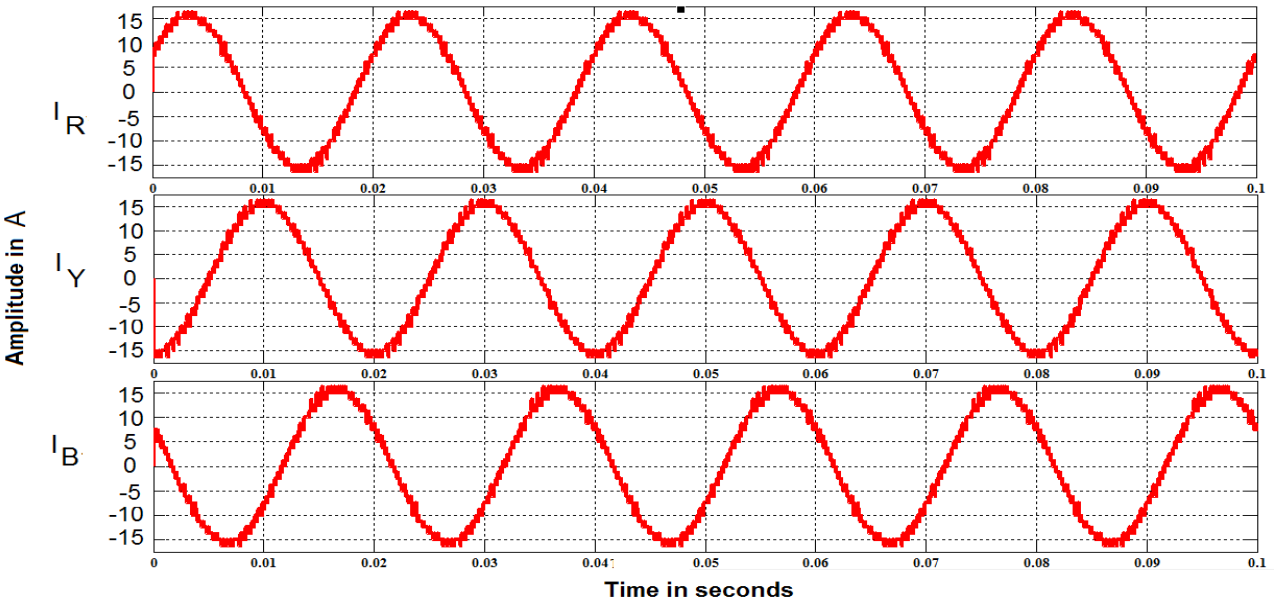

Figure 7. 3-phase line currents generated by VFPWM strategy for the proposed inverter

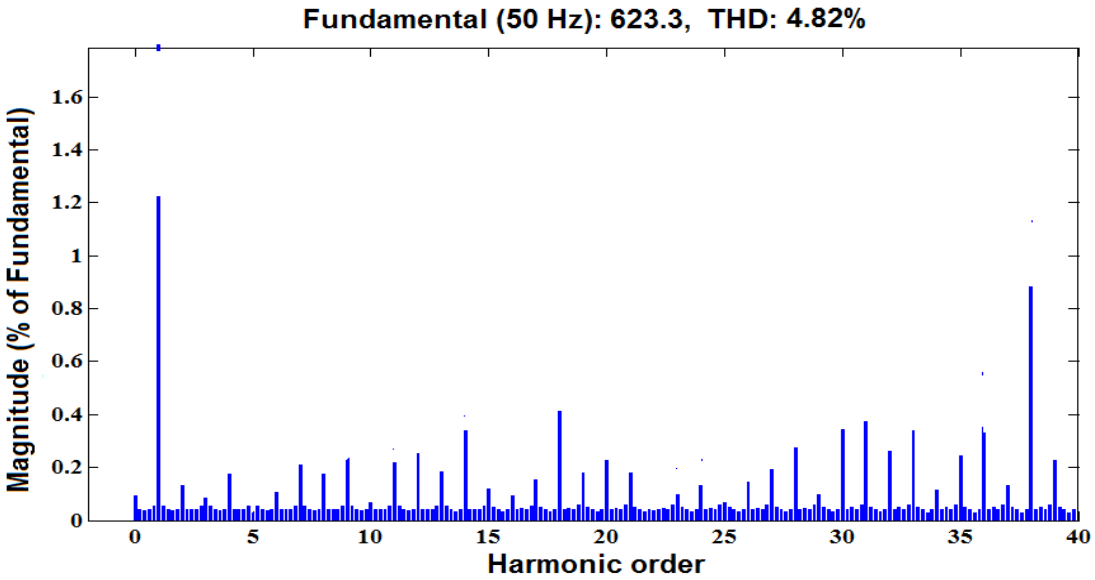

Figure 8. Harmonics present in 3-phase line currents produced by VFPWM method

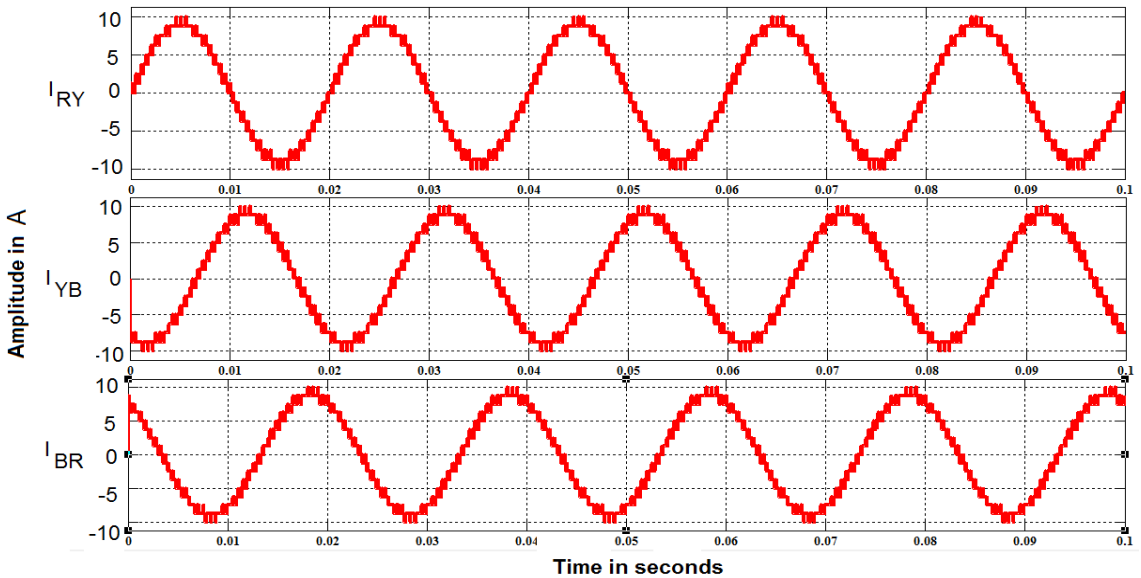

Figure 9. 3-phase currents generated by VFPWM strategy for the proposed inverter

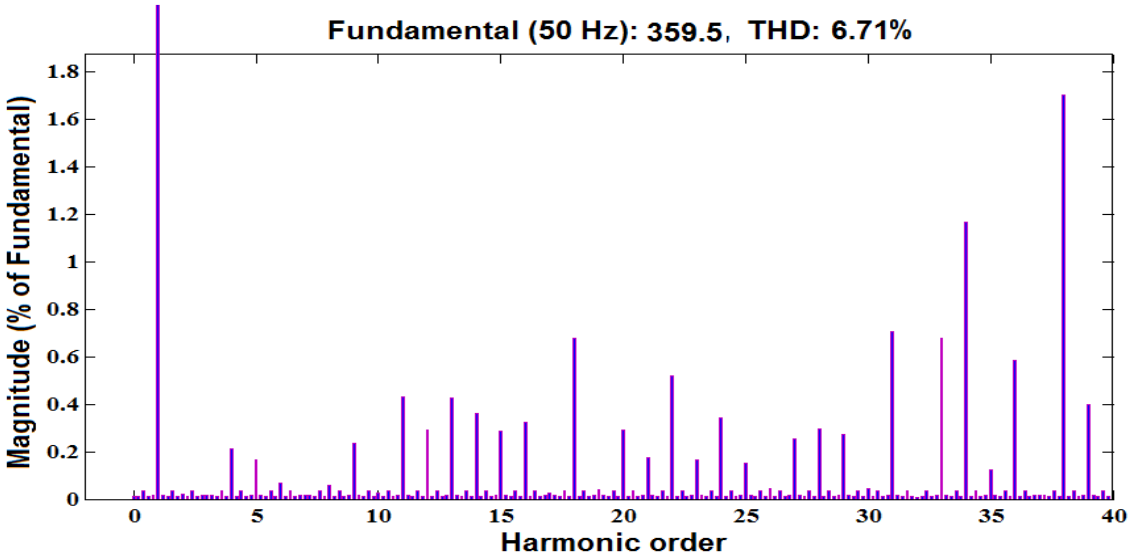

Figure 10. Harmonics present in 3-phase currents produced by VFPWM method

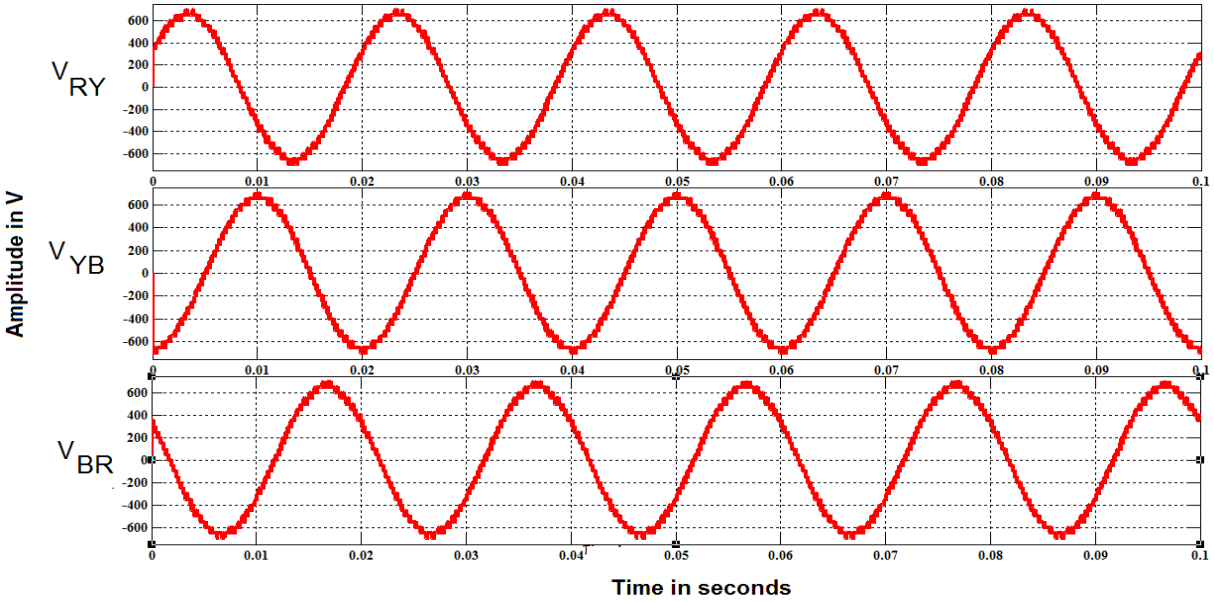

Figure 11. 3-phase line voltages generated by COPWM strategy for the proposed inverter

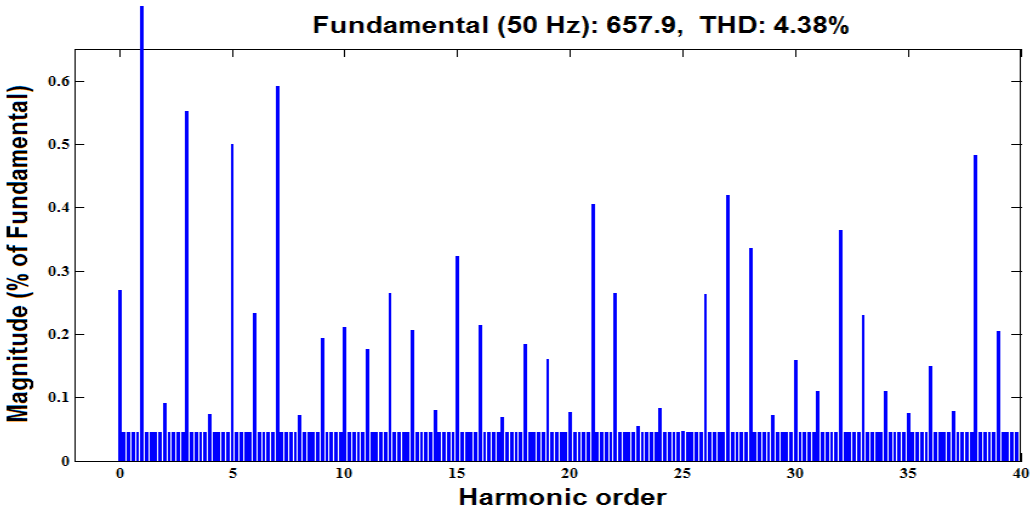

Figure 12. Harmonics present in 3-phase line voltages produced by COPWM scheme

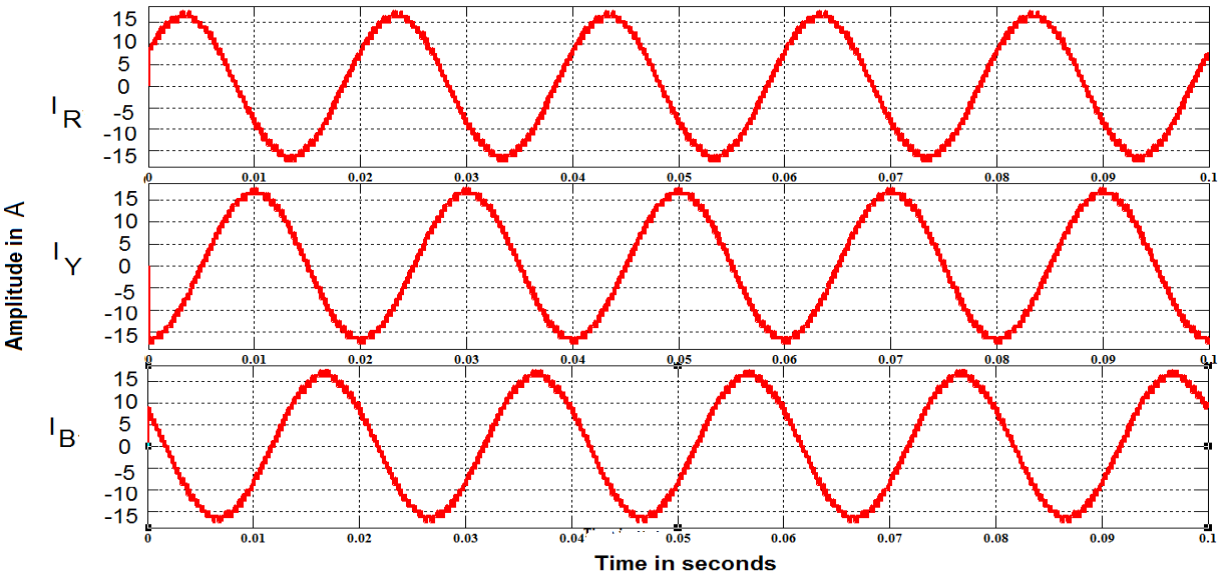

Figure 13. 3-phase line currents generated by COPWM strategy for the proposed inverter

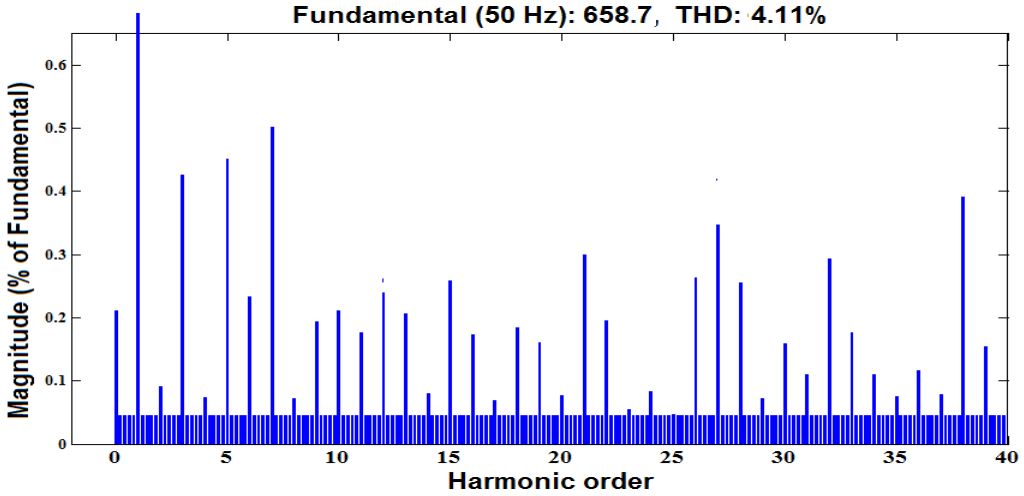

Figure 14. Harmonics present in 3-phase line currents produced by COPWM method

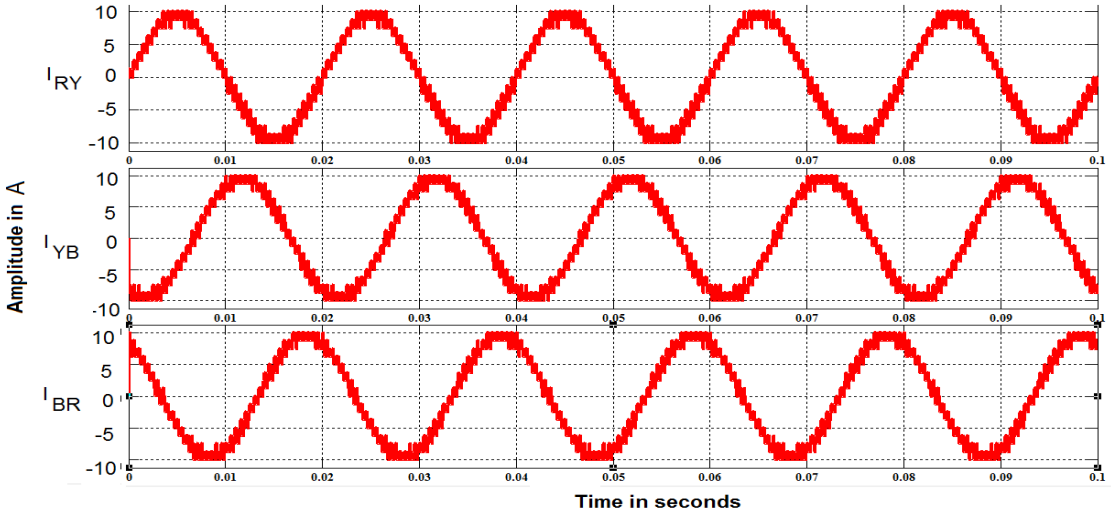

Figure 15. 3-phase currents generated by COPWM strategy for the proposed inverter

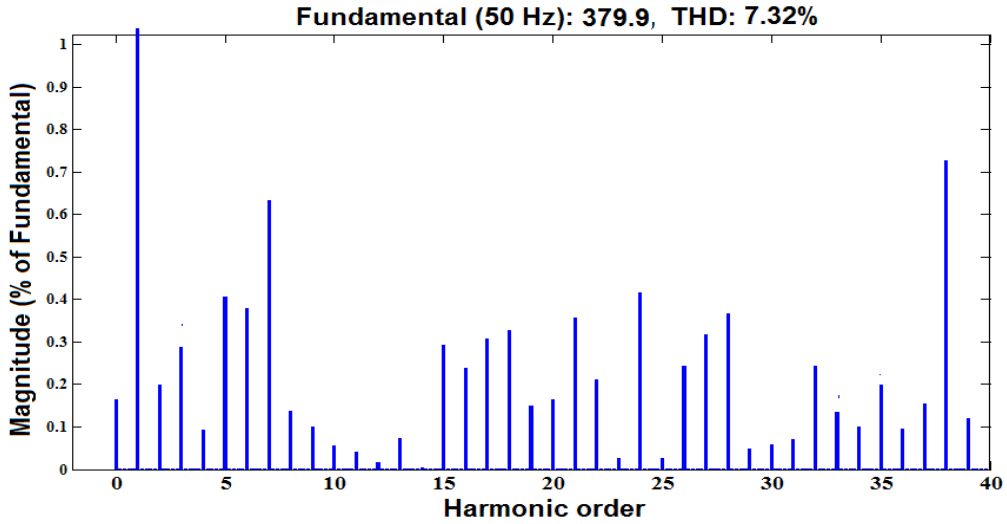

Figure 16. Harmonics present in 3-phase currents produced by COPWM method

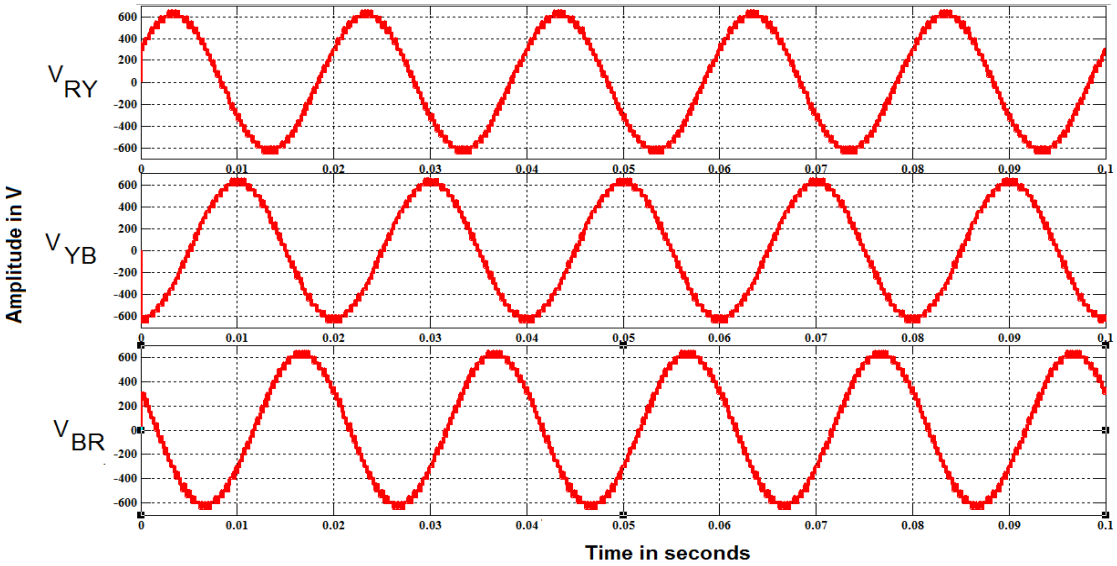

Figure 17. 3-phase line voltages produced by PDPWM strategy for the proposed inverter

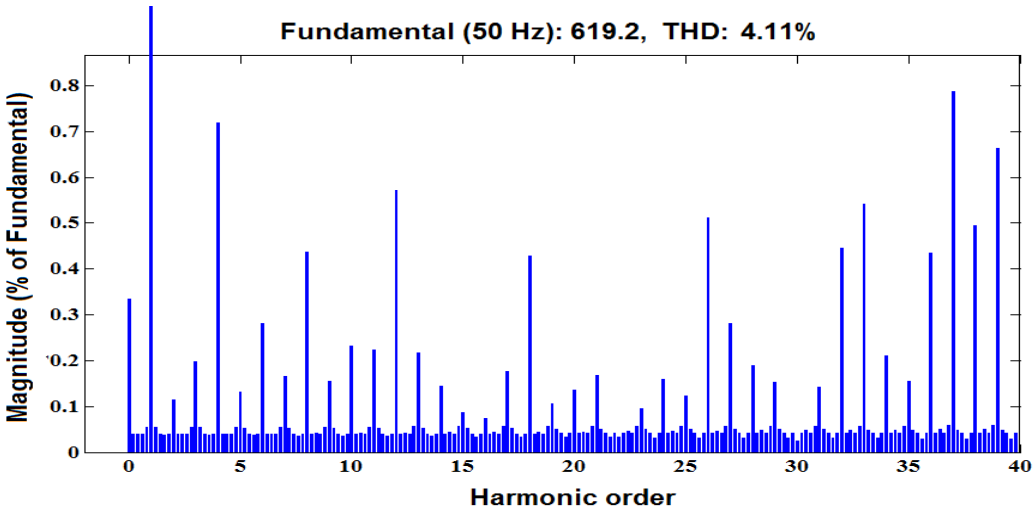

Figure 18. Harmonics present in 3-phase line voltages produced by PDPWM scheme

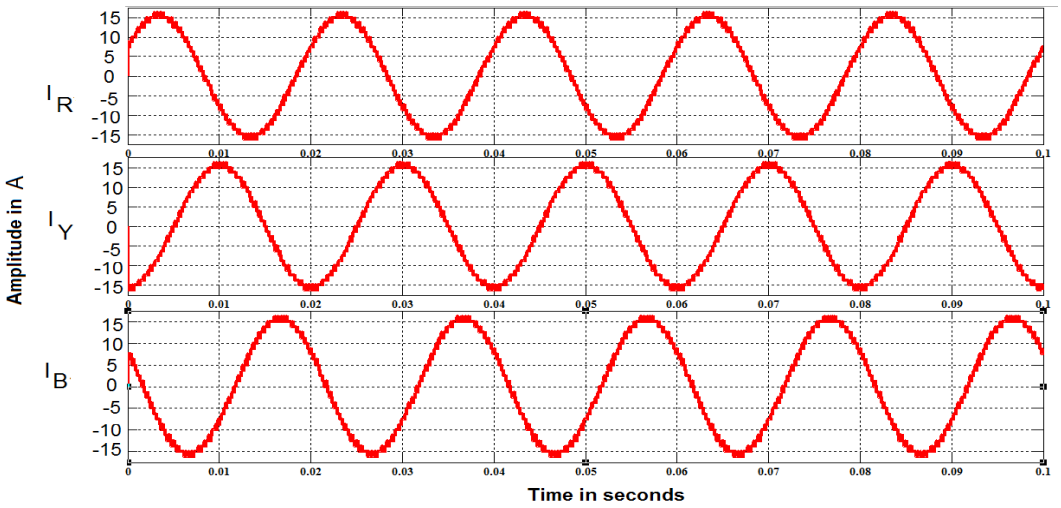

Figure 19. 3-phase line currents generated by PDPWM strategy for the proposed inverter

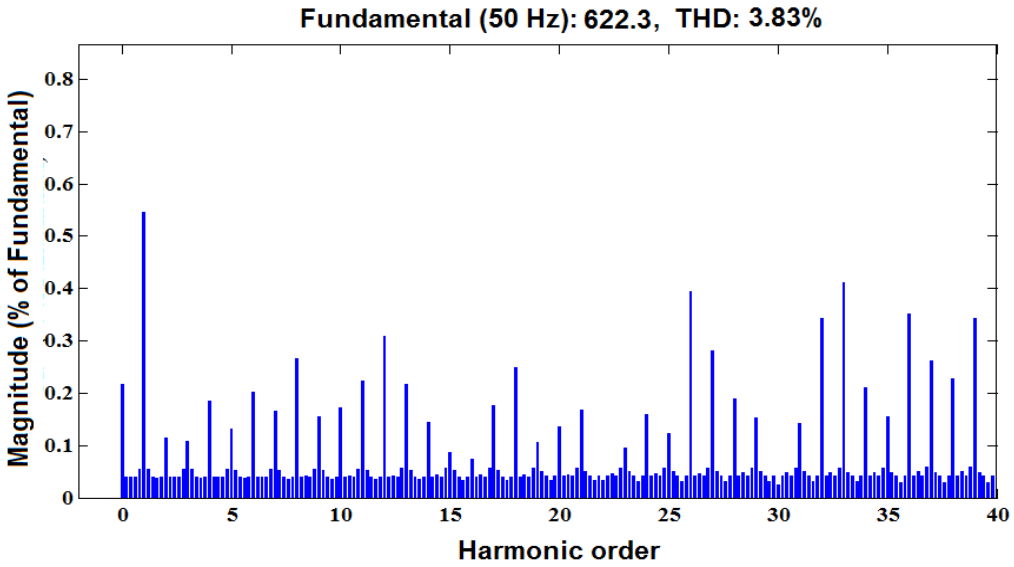

Figure 20. Harmonics present in 3-phase line currents produced by PDPWM method

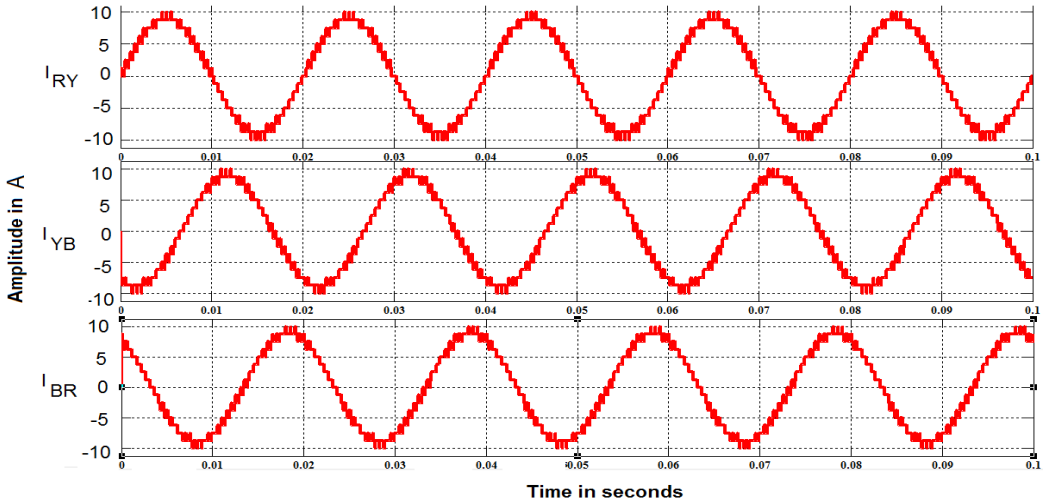

Figure 21. 3-phase currents generated by PDPWM strategy for the proposed inverter

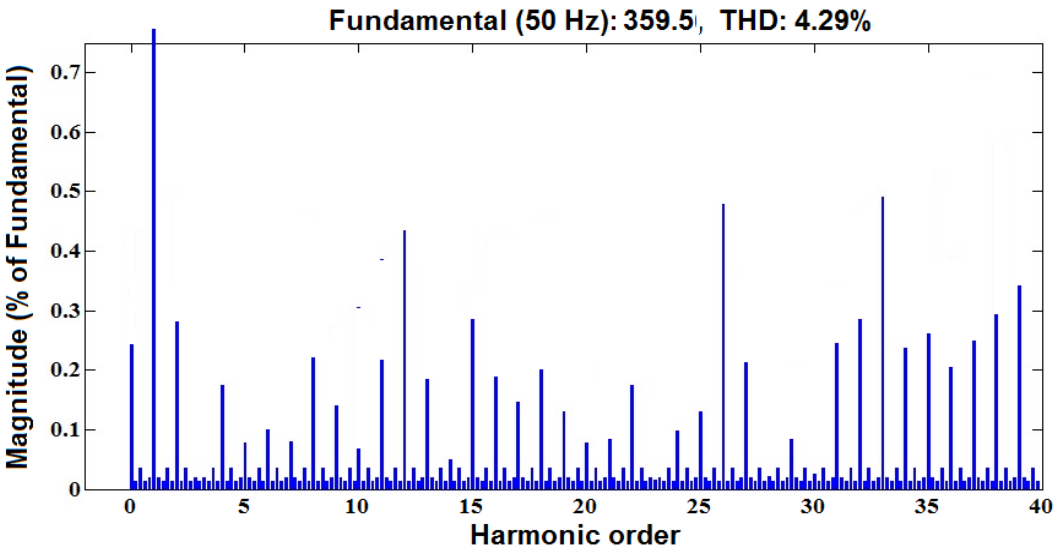

Figure 22. Harmonics present in 3-phase currents produced by PDPWM method

Table 3 Comparison of PDPWM, VFPWM, and COPWM strategies for the proposed 17-level inverter supplying a resistive load of 60 Ω / phase

Performance factors of the proposed 17-level inverter	Sinusoidal PWM schemes					
	PDPWM		VFPWM		COPWM	
	m_a = 0.85	m_a = 1	m_a = 0.85	m_a = 1	m_a = 0.85	m_a = 1
%THD for output voltage	4.11	4.01	5.91	4.98	4.38	4.29
RMS output voltage (V)	438	452	441	453	460	478
Peak output voltage (V)	620	639	624	641	650	676
%THD for output phase current	4.29	3.35	6.71	5.98	7.32	6.03
%THD for output line current	3.83	3.10	4.82	4.27	4.11	3.86
RMS output phase current (A)	7.30	7.53	7.35	7.55	7.67	7.97
RMS output line current (A)	12.64	13.04	12.73	13.08	13.28	13.80
Switching loss/phase (W)	0.092	0.117	0.093	0.120	0.097	0.128

Table 4 Variation of Switching loss and %THD for the proposed 17-level inverter controlled by PDPWM, VFPWM, and COPWM schemes with m_a = 0.85

Switching frequency (f_{SW}) kHz	Switching loss/phase (W)			%THD of voltage			%THD of line current			%THD of phase current		
	PD PWM	VF PWM	CO PWM	PD PWM	VF PWM	CO PWM	PD PWM	VF PWM	CO PWM	PD PWM	VF PWM	CO PWM
2	0.092	0.093	0.097	4.11	5.91	4.38	3.83	4.82	4.11	4.29	6.71	7.32
4	0.184	0.186	0.194	4.01	5.73	4.27	3.75	4.71	4.01	4.12	6.62	7.21
6	0.276	0.278	0.290	3.83	5.24	4.12	3.62	4.62	3.89	4.01	6.53	7.02
8	0.369	0.371	0.387	3.78	4.95	3.91	3.51	4.54	3.78	3.92	6.46	6.93
10	0.460	0.464	0.484	3.63	4.83	3.83	3.44	4.41	3.64	3.84	6.37	6.85

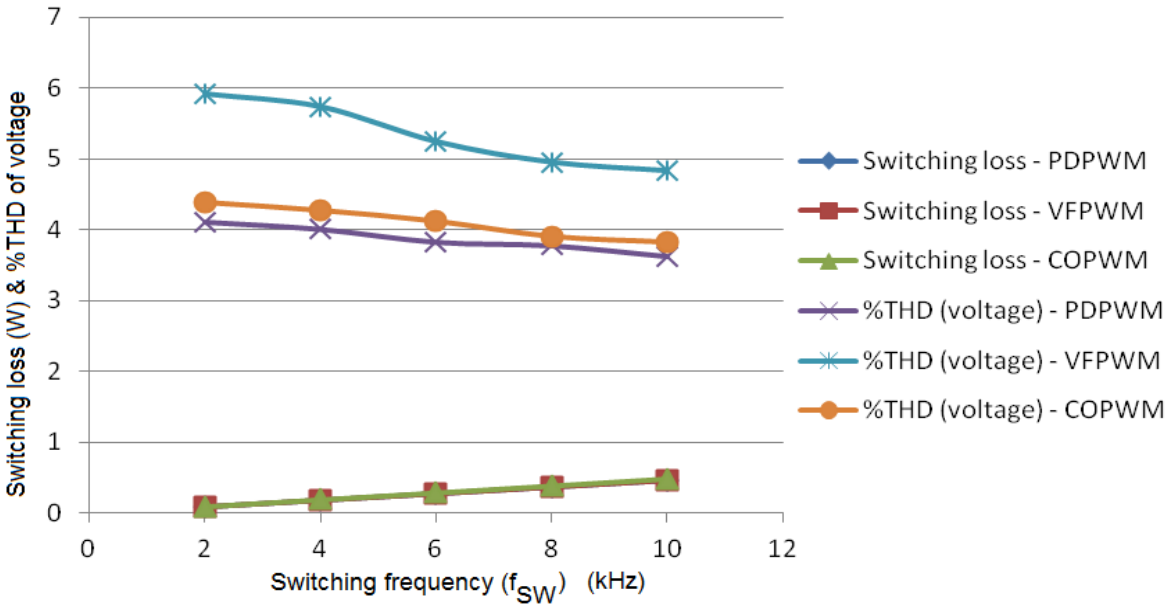

Figure 23. Variation of Switching loss and %THD of voltage with switching frequency

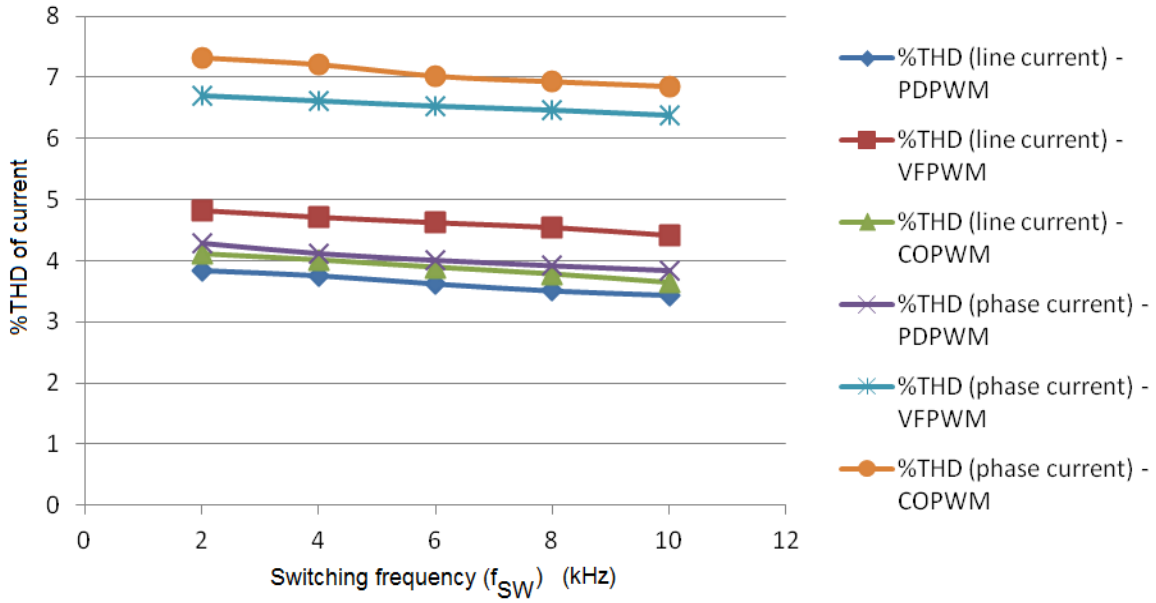

Figure 24. Variation of %THD of line and phase currents with switching frequency

CONCLUSION

In this research article, the VFPWM, COPWM, and PDPWM schemes are applied to the proposed 3-phase multilevel inverter capable of producing 17-levels of output voltages with less number of power switches. The effectiveness of the sinusoidal modulation strategies employed in this work is validated by testing the proposed inverter in Matlab/Simulink environment. The results demonstrate that the sinusoidal modulation methods have significantly improved the performance characteristics of the inverter in the form of higher output AC voltages with reduced harmonic content. The inverter performance is validated with various performance indices. It is evident from the simulation waveforms that the inverter implemented with phase disposition PWM scheme is able to produce output voltages and currents with lower amount of harmonic distortion of 4.11% in voltage, 4.29% in phase current, and 3.83% in line current, compared to other PWM schemes, and the inverter controlled by carrier overlapping technique is capable to generate output AC voltages of around 650 V (peak) and 460 V (RMS) compared with other PWM methods employed in the proposed work. The lower amount of around 0.092 W/phase switching loss is observed at the operation of the proposed inverter with phase disposition PWM method, at 2 kHz switching frequency. Further, it is also observed that significantly reduced harmonic distortion and higher values of output voltages are obtained by choosing amplitude modulation index parameter (m_a) nearer to 1. Hence, the

sinusoidal PWM techniques may be appropriately chosen as per the requirement of performance parameters, to suit the particular application of the inverter. However, the proposed inverter structure requires eight number of DC voltage sources in isolated configuration for each phase.

Funding: This research received no external funding.
Acknowledgments: The author acknowledges the technical support provided by the Department of Electrical and Electronics Engineering, Government College of Engineering, Tiruchirappalli, in carrying out the simulation work on the proposed inverter.
Conflicts of Interest: The author declares no conflict of interest.

REFERENCES

1. Balamurugan CR, Natarajan SP, Bensraj R, Shanthi B. A review on modulation strategies for multilevel inverter. Indones J Electr Eng Comput Sci, 2016 Sep; 3(3):681-705.
2. Rodriguez J, Sheng Lai J, Peng FZ. Multilevel inverters - a survey of topologies, controls and applications. IEEE Trans Ind Electron, 2002 Aug; 49(4):724-38.
3. Somasekhar VT, Baiju MR, Gopakumar K. Dual two-level inverter scheme for an open-end winding induction motor drive with a single DC power supply and improved DC bus utilization. IEE Proc – Electr Power Appl, 2004 Apr; 151(2):230-38.
4. Rawa M, Prem P, Mohamed Ali JS, Siddique MD, Mekhilef S, Wahyudie A,. A new multilevel inverter topology with reduced DC sources. Energies, 2021 Aug; 14(15):1-21.
5. Narendra kumar M, Rajanand Patnaik N, Subbarao M. Performance analysis of nested multilevel inverter topology for 72V electric vehicle applications. J Eur Syst Autom, 2020 Dec; 53(6):925-30.
6. Li R, Adam G, Holliday D, Fletcher JE, Williams B. Hybrid cascaded modular multilevel converter with DC fault ride-through capability for the HVDC transmission system. IEEE Trans Power Deliv, 2015 Aug; 30(4):1-10.
7. AI-Samawi AA, Trabelsi H. New nine-level cascade multilevel inverter topology with a minimum number of switches for PV systems. Energies, 2022 Aug; 15(16):1-25.
8. Ramu V, Satish Kumar P, Srinivas GN. LSPWM, PSPWM and NLCPWM on multilevel inverters with reduced number of switches. Mater Today, 2022 Mar; 54(3):710-27.
9. Gupta KK, Jain S. A new topology for multilevel inverter considering its optimal structures. Electric Power Syst Res, 2013 Oct; 103:145-56.REf
10. Masoudina F, Babaei E, Sabahi M, Alipour H. New cascaded multilevel inverter with reduced power electronic components. Iranian J Electr Electron Eng, 2019 Nov; 16(1):107-13.
11. Sivamani S, Mohan V. A three-phase reduced switch count multilevel inverter topology. Int Trans Electr Energy Syst, 2022 Dec; 2022:1-16.
12. Mahato B, Majumdar S, Chandra Jana K. Carrier-based PWM techniques for multi-level inverters: A comprehensive performance study. Gazi Univ J Sci. Part A: Engineering and Innovation, 2018 Sep; 5(3):101-11.
13. Tackie SN, Babaei E. Modified topology for three-phase multilevel inverters based on a developed H-bridge inverter. Electronics, 2020 Nov; 9(11):1-17.
14. Sengolrajan T, Balamurugan CR, Shanthi B. Simulation assessment of PWM strategies for three phase trinary source nine level inverter with rectified sine carriers. Int J Sci Eng Res, 2018 Mar; 9(3):145-56.
15. Banaei MR, Salary E. New multilevel inverter with reduction of switches and gate driver. Energy Convers Manag, 2011 Feb; 52(2):1129-36.
16. Siahbalaee J, Sanaie N. Comparison of conventional and new cascaded multilevel inverter topologies based on novel indices. ISA Trans, 2022 Jan; 119:41-51.
17. Ajami A, Oskuee MRJ, Mokhberdoran A, den Bossche AV. Developed cascaded multilevel inverter topology to minimize the number of circuit devices and voltage stresses of switches. IET Power Electron, 2014 Feb; 7(2):459-66.
18. Dhanamjayulu C, Prasad D, Padmanaban S, Maroti PK, Holm-Nielsen JB, Blaabjerg F. Design and implementation of seventeen level inverter with reduced components. IEEE Access, 2021 Feb; 9:16746-60.
19. Chaturvedi PK, Jain S, Agrawal P, Nema RK, Sao KK. Switching losses and harmonic investigations in multilevel inverters. IETE J Res, 2008 Aug; 54(4):295-305.
20. Farooq A, Tu S, Ahmad F, Malik MZ, Rehman OU, Hafeez G, ur Rehman S. A seventeen multilevel high-power application inverter with low harmonic distortion. Int J Photoenergy, 2021 Sep; 2021:1-17.
21. Chamarthi PK, Agarwal V, AI-Durra A. A new 1-Φ, seventeen level inverter topology with less number of power devices for renewable energy application. Front Energy Res, 2020 Jul; 8:1-13.