Morphological Study of Polycrystalline SiGe Alloy Deposited by Vertical LPCVD

R. C. Teixeira[1,2], I. Doi[1,2], J. A. Diniz[1,2], J. W. Swart[1,2], and M. B. P. Zakia[2]
[1]*School of Electrical and Computer Engineering (FEEC), State University of Campinas (UNICAMP), P.O. Box. 6101, CEP 13081-970, Campinas-SP, Brazil and*
[2]*Center for Semiconductor Components (CCS), State University of Campinas (UNICAMP), P.O. Box 6061, CEP 13083-870, Campinas-SP, Brazil*

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As device dimensions shrink to the deep-submicron scale, new challenges arises from the very small scale used and even poly crystalline silicon (poly-Si) presents problems as gate electrode. The use of SiGe as gate material can present many advantages over the poly-Si, as it leads to a lower boron penetration and gate depletion. In this paper authors present some morphological studies of polycrystalline SiGe thin films deposited in a vertical LPCVD (Low Pressure Chemical Vapor Deposition) reactor for using as MOS (Metal Oxide Semiconductor) gate electrode.

Keywords: Morphological study; Polycrystalline SiGe alloy; Low Pressure Chemical Vapor Deposition

I. INTRODUCTION

Polycrystalline-$Si_{1-x}Ge_x$ (poly-SiGe) alloys have been studied for microelectronics devices during the last 30 years [1-3] to allow deep submicron MOS fabrication [1], bipolar transistors and optical devices [3]. Many advantages emerge from the usage of poly-SiGe as gate electrode for MOS devices, such as lower power consumption, higher boron activation, no gate depletion and lower resistivity [1,3]. Different Ge fractions in the alloy lead to the so-called engineering workfunction that eliminates the need of channel implantation to achieve the desirable Threshold Voltage [1,3]. The low thermal budget used for the alloy deposition also makes poly-SiGe quoted as a material for MEMS (Micro Electro Mechanical Systems) application [4].

In this study authors present morphological studies of poly-SiGe deposited in a vertical LPCVD epitaxial reactor over oxidized single crystalline silicon wafers. We analyze grain size, surface rms roughness and preferred orientation by means of AFM (Atomic Force Microscopy), XRD (X-Ray Diffraction) and SEM (Scanning Electron Microscopy) measurements. RBS (Rutherford Backscattering Spectroscopy) analysis shows that Ge fractions up to 32% are achieved in this parameter window.

We found that a strong $< 111 >$ preferred orientation (PO) is obtained for samples deposited at 750 $^\circ$C for both 5 and 10 Torr deposition pressure and that the films are formed by agglomerates a few hundreds nanometers large with smaller structures some tenth's nanometers large inside. It also shows some twinning and that the grain size increases with temperature, like poly-Si thin films. Surface rms roughness as low as 4 nm was observed in the AFM scans.

II. EXPERIMENTAL

Poly-SiGe thin films were deposited by LPCVD in a Pancake Vertical Reactor onto 100 Å thermally dry oxidized $< 100 >$, n-type, 1-10 Ω.cm single crystalline silicon substrates. Precursor gases were silane and germane in a hydrogen carrier gas flow. All gases have 5.0 purity. Deposition temperature ranged from 500 to 750 $^\circ$C, with 50 $^\circ$C steps, at 5 or 10 Torr pressure, measured by an infrared pyrometer.

Thickness and Ge fraction were extracted from RBS (He ions, 2.2 MeV) measurements. XRD (Fe radiation) in the theta-2theta configuration was used to verify the internal structure of the obtained samples while morphological aspects were analyzed by means of AFM and SEM.

III. RESULTS AND DISCUSSION

RBS analysis with the RUMP software package allows the measurement of both thickness and Ge contents (x) in the poly-SiGe samples. Results are shown in Fig. 1 below.

Deposition rates as high as 1500 Å/min were achieved for both 5 and 10 Torr samples. The temperature range used in this study leads to process limited by reaction rate, as one can note by the great influence of temperature on the deposition rate. As expected, 10 Torr pressure presents a slightly higher deposition rate as the higher pressure employed leads to a higher precursor concentration. This reflects in a lower activation energy (Ea) compared with the 5 Torr set (1.13 eV and 1.20 eV for 10 and 5 Torr respectively). These Ea values also justify the low deposition temperature range compared to the poly-Si deposition window. Poly-Si deposition process are reported to have activation energy between 1.6 and 2.0 eV and previous studies show that 700 $^\circ$C is the minimum temperature for poly-Si thin film deposition in this reactor, using similar flow and pressure conditions. From Fig. 1 – top we can also notice that the films obtained at 10 Torr present saturation on the deposition rate at 750 $^\circ$C. This is related to the transition from the reaction rate limited to the mass transport limit.

Temperature also gives rise to differences in the Ge contents (x) in the alloy (Fig. 1- bottom). The x value rises up to a maximum of 31% at 650 $^\circ$C and 37% at 600 $^\circ$C for 5 and 10 Torr, respectively. The initial increase in the Ge contents is

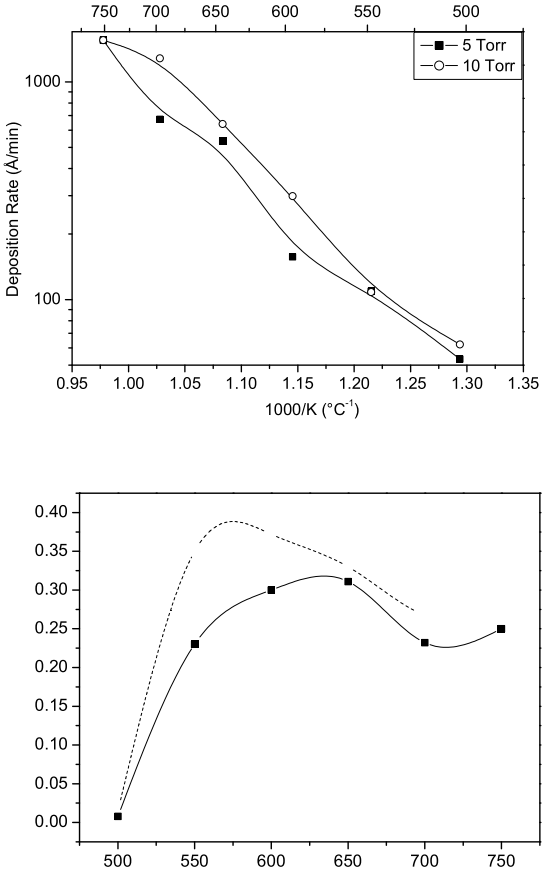

FIG. 1: Deposition rate (top) and Ge fraction (bottom) as a function of deposition temperature as calculated from RBS measurements.

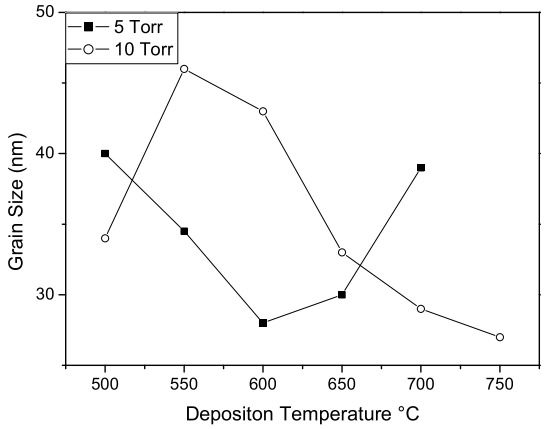

FIG. 2: Grain Size of poly-SiGe films.

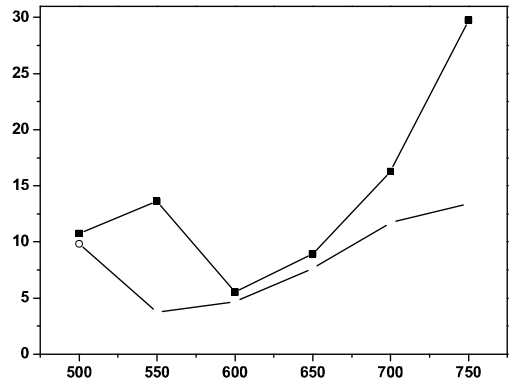

FIG. 3: RMS surface roughness of poly-SiGe films.

an effect of temperature solely, as more energy is delivered to the system, enhancing the Ge adsorption/deposition. As the temperature reaches the limit of the Si deposition (600 ˚C for the amorphous phase in this reactor), the Ge content reduces due to the Si incorporation to about 25%. The variation in Ge contents does not seem to influence the deposition rate.

Deposition parameters also affect grain size as shown in Fig. 2, but this characteristic presents no relation to the deposition rate and Ge fraction.

On the other hand, the rms surface roughness (SR) presents a simpler, parabolic behaviour for both pressures (Fig.3). The minimum SR values obtained were 5.53 nm at 600 ˚C and 3.73 nm at 550 ˚C for 5 and 10 Torr respectively.

The increase in the surface roughness is related to the presence of the $< 111 >$ oriented grains as pointed by XRD measurements (Fig. 4). This orientation is expected for high deposition temperatures, as 4 atoms are needed to nucleate in the $< 111 >$ direction, i.e., more energy is needed to form the necessary bindings to occur the nucleation. These grains also need two layers of Si/Ge atoms to grow. Thus, the higher the $< 111 >$ intensity and the bigger the grain size, the higher the SR will be, as one can notice comparing SR values of samples deposited at 750 ˚C on Figs. 3 and data of Figs. 2 and 4.

The $< 220 >$ grains need just one layer and 2 atoms to nucleate so it is preferred at lower temperatures, as observed in the Fig. 4. These grains are smoother than the $< 111 >$ ones, so that samples with a bigger $< 220 >$ orientation have a lower SR. These assumptions justify the lower roughness observed for all films deposited at 10 Torr. These samples always presented a $< 220 >$ resonance proportionally bigger than the $< 111 >$ resonance than samples deposited at 5 Torr.

AFM and SEM images (Fig. 5) also presented agglomerates a few hundreds nm large formed by smaller structures some tenth's nm large. Grain size ranges from 27 up to 46 nm, however, we can note some not well defined boundaries of smaller grains embedded on larger grains that may be related to twinnings, probably due to the high deposition rate obtained.

To verify the ability of this material on MOS fabrication, another set of MOS capacitors was also prepared using ultrathin silicon oxinitride SiON) grown by ECR (Electron Cyclotron Resonance) Plasma at ambient temperature as gate dielectric. The poly-SiGe film was obtained at 5 Torr / 500 ˚C and the samples, sintered at 450 ˚C in a forming gas ambi-

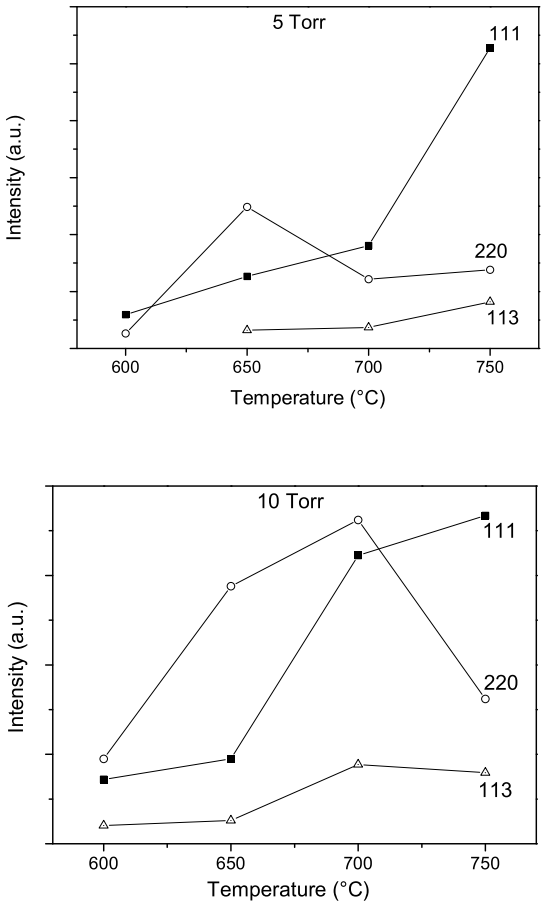

FIG. 4: Intensity of the resonance peaks for 5 (top) and 10 (bottom) Torr samples.

ent during 30 min, and no metal deposition was used. From the CxV (Figure 6) and IxV measurements we obtain Equivalent Oxide Thickness (EOT) of 3.2 nm and a leakage current of 6 mA/cm^2 (Vgs = -1V), respectively. Figure 6 also shows that the measurements are in a very good agreement with data simulated by CVC software.

IV. CONCLUSION

Poly-SiGe thin films were obtained in the vertical LPCVD system on very high deposition rates, up to 1500 Å/min. Samples presented agglomerates of small crystalline grains from 27 to 49 nm in diameter and rms surface roughness with a parabolic behavior. The SR increases with the $< 111 >$ grain orientation. CxV measurements are very promising and are in good agreement with CVC simulation. A very low leakage current was observed for capacitor fabricated onto SiON dielectrics

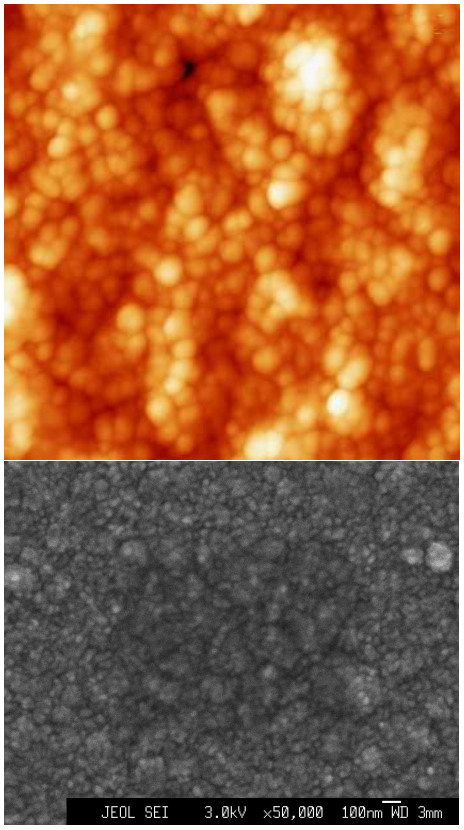

FIG. 5: AFM (top) and SEM (bottom) images of poly-SiGe show agglomerates formed by smaller grains.

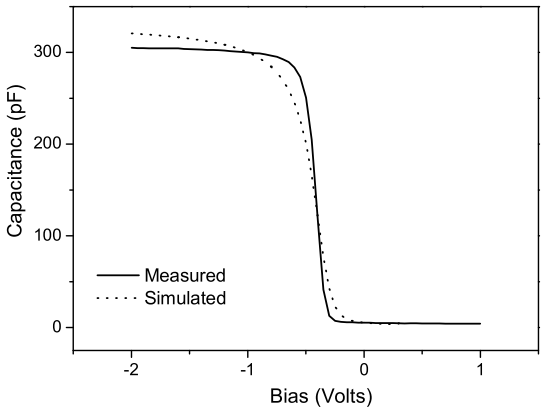

FIG. 6: CxV characteristics of MOS capacitors with poly-SiGe as gate electrode and SiON as gate dielectric.

V. ACKNOWLEDGEMENT

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