A LINE-INTERACTIVE UPS SYSTEM IMPLEMENTATION WITH SERIES-PARALLEL ACTIVE POWER-LINE CONDITIONING FOR THREE-PHASE, FOUR-WIRE SYSTEMS

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Abstract

This paper presents a three-phase line-interactive uninterruptible power supply (UPS) system with active series-parallel power-line conditioning capabilities. Synchronous reference frame (SRF)-based controller is used for harmonic and reactive power compensation generated from any configuration of non-linear loads. Under normal line conditions the UPS system works with universal filtering capabilities, such as compensating the input currents and output voltages. Two three-phase pulsewidth modulation (PWM) converters, called series and parallel active filters, are used to perform the series and parallel active power-line compensation. The series active filter works as sinusoidal current source in phase with the input voltage, drawing from utility sinusoidal and balanced input currents with low total harmonic distortion (THD). The parallel active filter works as sinusoidal voltage source in phase with the input voltage, providing regulated and sinusoidal output voltages with low THD. The performance of the UPS system is evaluated in three-phase, four-wire systems. Experimental results are presented to confirm the theoretical studies.

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Resumo

Este artigo apresenta um sistema de energia ininterrupta (SEI) *line-interactive* trifásico com capacidade de condicionamento ativo de potência série e paralelo. Um controlador baseado no sistema de eixo de referência síncrona (SRF) é usado na compensação de potência reativa e harmônica geradas por quaisquer configurações de cargas não lineares. Sob condições normais da rede elétrica o SEI trabalha na compensação das correntes de entrada e das tensões de saída. Dois conversores controlados em tensão e modulados por largura de pulso (PWM), chamados de filtros ativos série e paralelo, são usados para realizar o condicionamento ativo de potência série e paralelo. O filtro ativo série trabalha como uma fonte de corrente senoidal em fase com a tensão de entrada, drenando da rede correntes senoidais, balanceadas com baixas taxas de distorção harmônica (TDH). O filtro ativo paralelo trabalha como uma fonte de tensão senoidal em fase com a tensão de entrada, fornecendo para a carga tensões reguladas, senoidais e com baixas taxas de distorção harmônica. O desempenho do SEI é avaliado para sistemas trifásicos com quatro fios. Resultados experimentais são apresentados para confirmar os estudos teóricos.

Palavras Chaves: Filtro ativo, SEI, Harmônicas.

1 INTRODUCTION

The large use of non-linear loads, such as, personal computers, UPS, etc., has increased in the last years, causing problems to the power supply systems. The harmonic currents drawn by non-linear loads from utility have contributed to reduce the power factor and to increase the total harmonic distortion (THD) in the utility input voltages. The problem increases when single-phase non-linear loads are connected in three-phase, four-wire systems. In this case, as the phase currents are not sinusoidal, even perfectly balanced single-phase loads can result in significant neutral currents and their amplitude can exceed the amplitude of the line currents (Gruzs, 1990). If the non-linear loads are unbalanced, the input currents will be unbalanced in terms of fundamental and harmonic components, and a very large third component and its multiples will flow in the neutral wire. The excessive neutral currents can cause damage both in the neutral conductor and in the transformer to which it is connected (Quinn *et al*., 1992). Thereby, active filter topologies have been used to compensate neutral harmonic currents (Quinn *et al*., 1992; Quinn *et al*., 1993; Thomas *el al*., 1996).

Uninterruptible power supply (UPS) systems have enabled the improvement of power source quality, providing clean and uninterruptible power to critical loads such as industrial process controls, computers, medical equipment, data communication systems, and protection against power supply disturbances or interruptions (Oliveira da Silva *et al*., 2001; Kamran *et al*., 1995; Jeon *et al*., 1997, Cheung *et al*., 1996; Lin *et al*., 1993). In (Lin *et al*., 1993) a three-phase parallel processing UPS has been presented with harmonic and reactive power compensation, but the output voltages and the input currents cannot be controlled simultaneously. Three-phase UPS systems with series-parallel active power-line conditioning have been proposed using different control strategies (Oliveira da Silva *et al*., 2001; Kamran *et al*., 1995). In (Kamran *et al*., 1995) the three-phase UPS system was employed for three-wire systems, and in (Oliveira da Silva *et al*., 2001), albeit it can be employed for three-wire and four-wire systems, the UPS was used to feed a non-linear load composed by a three-phase non-controlled rectifier, in which neutral currents do not exist.

This paper presents a three-phase line-interactive UPS system with active series-parallel power-line conditioning capabilities using an SRF-based controller, for three-wire and four-wire systems in which three single-phase loads are fed. In UPS standby operation mode, the series active power filter acts as a sinusoidal current source and the parallel active power filter acts as a sinusoidal voltage source (Oliveira da Silva *et al*., 2001). The output voltages are controlled to have constant rms values and low THD and the source currents are controlled to be sinusoidal and balanced with low THD. Both input currents and output voltages are simultaneously controlled to be in phase with respect the input voltages. Therefore, an effective power factor correction is carried out.

The control algorithm using SRF method and the active power flow through the UPS system are described and analytically studied. Design procedures, digital simulations and experimental results for a prototype are presented in order to verify the good performance of the proposed three-phase line-interactive UPS system.

2 DESCRIPTION OF THE LINE-INTERACTIVE UPS TOPOLOGY

The topology of the line-interactive UPS system is shown in Fig. 1. Two pulsewidth modulation (PWM) converters, coupled to a common dc-bus, are used to perform the series active filter and the parallel active filter functions. Capacitors and a battery bank are placed in the dc-bus and a static switch 'sw' is used to provide the disconnection between the UPS system and the power supply when an occasional interruption of the incoming power occurs. The center-tap of the dc-bus is connected to the utility neutral.

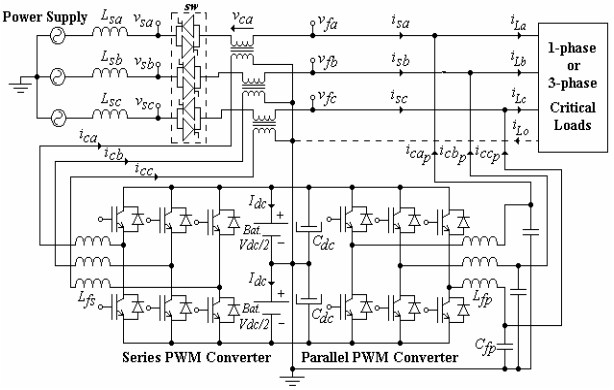


Figure 1. Line-Interactive UPS system topology

3 SYNCHRONOUS REFERENCE FRAME AND STATE FEEDBACK CONTROLLERS

3.1 Current SRF-Based Controller (Standby Mode)

An SRF-based controller is used to provide and to control the compensating reference currents (i_{ca}^{*}, i_{cb}^{*}, and i_{cc}^{*}) for the series PWM converter shown in Fig. 1. The block diagram of the control scheme for current compensation is shown in Fig. 2. The three-phase load currents (i_{La}, i_{Lb}, i_{Lc}) are measured and transformed into a two-phase stationary reference frame $(dq)^{s}$ quantities (id^{s}, iq^{s})

based on the transformation (1). Then, these quantities are transformed from a two-phase stationary reference frame $(dq)^s$ into a two-phase synchronous rotating $(dq)^e$ reference frame, based on the transformation (2), where $\theta = \omega t$, is the angular position of the reference frame. The unit vectors $sin\theta$ and $cos\theta$ are obtained from PLL system. The currents at the fundamental frequency ω (id^e and iq^e) are now dc values and all the harmonics, transformed into non-dc quantities, can be filtered using a low pass filter (LPF) as shown in Fig. 2. Now, id^e_{dc} represents the fundamental active component of the load current and iq^e_{dc} represents the fundamental reactive component of the load current, both in dq axis.

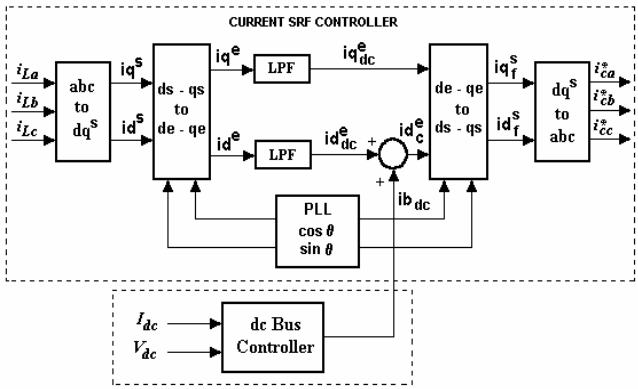


Figure 2. Block diagram of the current SRF-based controller.

An additional dc-bus controller is responsible for regulating the current I_{dc} and the voltage V_{dc}. Apart from the conventional active filter applications, in which only the dc-bus voltage is controlled, the UPS dc-bus controller is able to control the dc-bus current for adequate charging of the battery bank. The dc-bus controller is also responsible to control the active power flow of the UPS system. Its output ib_{dc} is added to the active current in the d axis id^e_{dc} as given by (3) and, thus, the amplitude of the reference currents can be controlled by id^e_c.

$$\begin{bmatrix} id^s \\ iq^s \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} id^e \\ iq^e \end{bmatrix} = \begin{bmatrix} \cos\theta & sin\,\theta \\ -sin\,\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^s \\ iq^s \end{bmatrix} \quad (2)$$

$$id^e_c = id^e_{dc} + ib_{dc} \quad (3)$$

Now, the dc components of the synchronous reference frame id^e_c and iq^e_{dc} can be transformed into the stationary reference frame $(dq)^s$. The inverse transformation matrix from two-phase synchronous reference frame to two-phase stationary reference frame is given by (4). As only the fundamental active component reference needs to be obtained, (4) can be replaced by (5).

The matrix that provides the linear transformation from two-phase system to three-phase stationary reference frame system is given by (6). Thereby, the dc component of the synchronous reference frame id^e_c is transformed into the stationary reference frame $(dq)^s$ and yields the fundamental components of the load currents (i^*_{ca}, i^*_{cb}, and i^*_{cc}). Such reference currents are generated in software.

$$\begin{bmatrix} id^s_f \\ iq^s_f \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\,\theta \\ sin\,\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^e_{dc} \\ iq^e_{dc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} id^s_f \\ iq^s_f \end{bmatrix} = \begin{bmatrix} \cos\theta & -sin\,\theta \\ sin\,\theta & \cos\theta \end{bmatrix} \begin{bmatrix} id^e_{dc} \\ 0 \end{bmatrix} \quad (5)$$

$$\begin{bmatrix} i^*_{ca} \\ i^*_{cb} \\ i^*_{cc} \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} id^s_f \\ iq^s_f \end{bmatrix} \quad (6)$$

3.2 State Feedback Current Controller (Standby Mode)

The single-phase block diagram of the current controller is shown in Fig. 3. The load currents ($i_{L\,a,b,c}$) are measured and from the current SRF controller the sinusoidal current references ($i^*_{c\,a,b,c}$) are obtained. From Fig. 3, the closed-loop transfer function $i_c(s)/i^*_c(s)$ is found as (7), in which the gain of the PWM block is one.

The dynamic stiffness transfer function of the series converter is given by (8), which is defined as the magnitude of the difference between the input and output voltages that

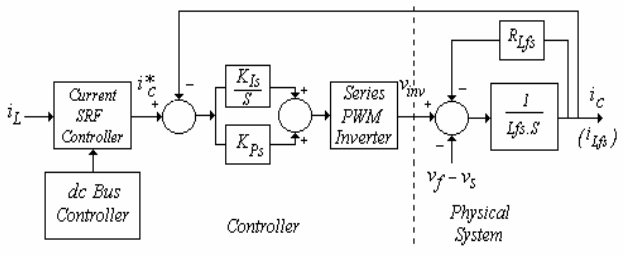


Figure 3. Single-phase current controller of the series active filter (series converter).

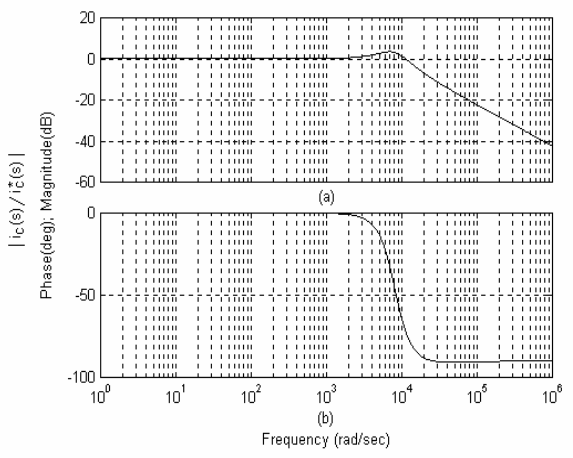


Figure 4. Frequency Response of the series active filter $i_c(s)/i_c^*(s)$:
(a) Amplitude response, (b) Phase response.

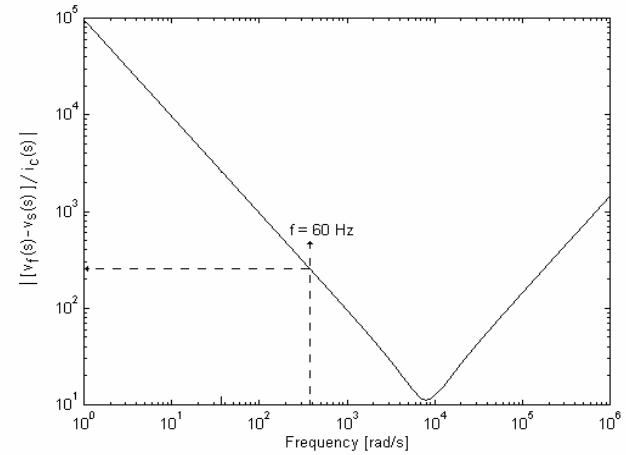


Figure 5. Dynamic Stiffness of Current Controller $\left|(v_f(s)-v_s(s))/i_c(s)\right|$: Frequency response.

causes a unit deviation in input current i_s (i_c): $\left|(v_f(s)-v_s(s))/i_c(s)\right|$. The voltage difference is considered as a disturbance.

Table 1 – Parameters and Controller Gains (Current Controller)

Series Filter Inductor, L_{fs}	1.4mH
Inductor Resistance, R_{Lfs}	0,05Ω
Proportional gain, K_{Ps}	11,21 Ω
Integral gain, K_{Is}	95231 Ω/s

$$\frac{i_c(s)}{i_c^*(s)} = \frac{K_{Ps}s + K_{Is}}{L_{fs}s^2 + (K_{Ps} + R_{L_{fs}})s + K_{Is}} \quad (7)$$

$$\frac{v_f(s) - v_s(s)}{i_c(s)} = -\frac{L_{fs}s^2 + (K_{Ps} + R_{L_{fs}})s + K_{Is}}{s} \quad (8)$$

The frequency response of equation (7) is shown in Fig. 4 (a) and (b). At the power system frequency (ω = 377 rad/s), the gain of the system transfer function is about 0 dB and the phase shift is nearly zero degree. The bandwidth of the system is about 1600 Hz. Fig. 5 shows the dynamic stiffness frequency response of the current controller. It can be noted high impedance obtained from (8) in a large range of the frequency spectrum, which is enough to isolate the line from the load with respect to current harmonics. The parameters and gains used to plot the curves of Figs. 4 and 5 are listed in Table 1.

3.3 State Feedback Voltage Controller (Standby and Backup Modes)

The parallel converter controls the output voltages to be in phase with the input voltages. Besides, the output voltages should be constant rms values with low THD. Similar to the control algorithm for input current compensation, the reference voltages ($v_{f\,a,b,c}^*$) are generated by software using a PLL system (Oliveira da Silva *et al*., 2001).

Fig. 6 shows the single-phase block diagram of the voltage controller, with an outer voltage loop and an inner current loop. To anticipate any errors to occur in the output voltage, a disturbance input decoupling is implemented by measuring the load current i_L and the source current i_s. The difference between them is used as an additional current loop command. Thus, only the capacitor current is used as a feedforward command ($i_{C_{fp}}^* = S\hat{C}_{fp}$). To simplify the control, such command was used only to plot the curves of Figs. 7 and 8 but it was not implemented in laboratory. From Fig. 6, the closed-loop transfer function

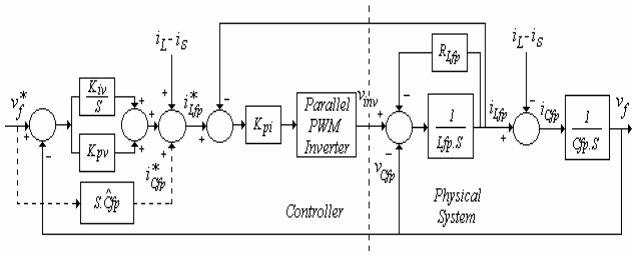


Figure 6. Single-phase voltage controller of the parallel active filter (parallel converter).

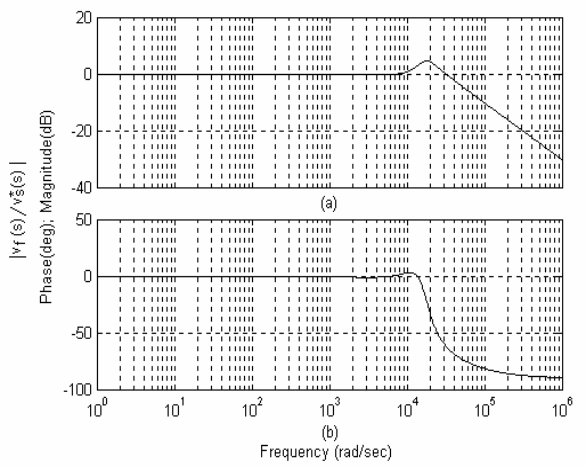


Figure 7. Frequency response of the parallel active filter $v_f(s)/v_f^*(s)$:
(a) Amplitude response, (b) Phase response.

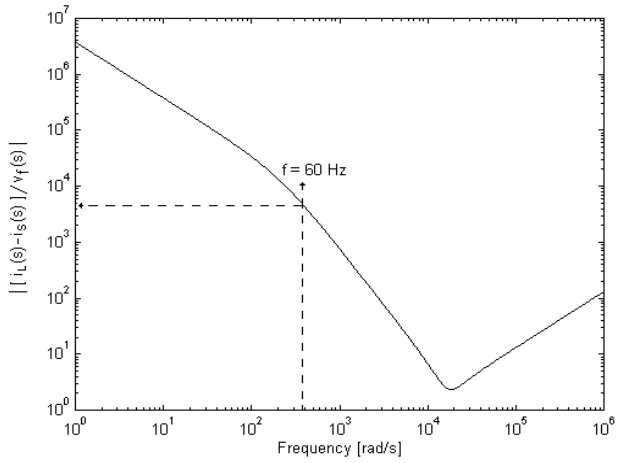


Figure 8. Dynamic Stiffness of Voltage Controller $\left|(i_L(s)-i_s(s))/v_f(s)\right|$: Frequency response.

$v_f(s)/v_f^*(s)$ is found as (9), in which the gain of the PWM block is one.

The dynamic stiffness transfer function of the parallel converter is given by (10), which is defined as the magnitude of the difference between the output and input currents that causes a unit deviation in output voltage v_f: $\left|(i_L(s)-i_s(s))/v_f(s)\right|$. The current difference is considered as a disturbance.

The coefficients X_n and Y_n of the equation (9) and (10) are given by (11).

$$\frac{v_f(s)}{v_f^*(s)} = \frac{X_1 s^2 + X_2 s + X_3}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \tag{9}$$

$$\frac{i_L(s)-i_s(s)}{v_f(s)} = -\frac{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4}{Z_1 s^2 + Z_2 s} \tag{10}$$

$$\left.\begin{array}{lll} X_1 = \hat{C}_{fp}.K_{Pi} & Y_1 = L_{fp}.C_{fp} & Z_1 = L_{fp} \\ X_2 = K_{pv}.K_{Pi} & Y_2 = C_{fp}.(K_{Pi} + R_{Lfp}) & Z_2 = R_{Lfp} \\ X_3 = Y_4 = K_{Iv}.K_{Pi} & Y_3 = K_{pv}.K_{Pi} + 1 & \end{array}\right\} \tag{11}$$

The frequency response of equation (9) is shown in Fig. 7 (a) and (b). At the power system frequency (ω = 377 rad/s), the gain of the system transfer function is about 0 dB and the phase shift is nearly zero degree. The bandwidth of the system is about 6000 Hz. Fig. 8 shows the dynamic stiffness frequency response of the voltage controller. It can be seen a high admittance obtained from (10) in a large range of the frequency spectrum, which is enough to absorb the harmonic currents of the load.

The parameters and gains used to plot the curves of Figs. 7 and 8 are listed in Table 2.

Table 2 – Parameters and Controller Gains (Voltage Controller)

Parallel Filter Inductor, L_{fp}	250μH
Inductor Resistance, R_{Lfp}	0,05Ω
Parallel Filter Capacitor, C_{fp}	130μF
Feed-Forward Capacitor, $\hat{C}_{fp}$	130μF
Proportional gain, K_{Pi}	7,85 Ω
Proportional gain, K_{Pv}	2,09 Ω^{-1}
Integral gain, K_{Iv}	24253 Ω^{-1}/s

3.4 Relation between the series $|Z_S|$ and the parallel $|Z_p|$ Impedances.

From Fig. 8, it can be noted that the higher impedance of the parallel converter occurs at 3 KHz ($|Z_{p\max}| = 0{,}4\Omega$). At this same frequency, from Fig. 5, the impedance of the series converter is $|Z_S| = 20\Omega$. Thus, the relation between $|Z_S|$ and $|Z_{p\max}|$ is approximately 50. This is enough for the parallel converter to absorb the harmonic currents of the load.

From Fig. 5 it can be seen that the lower series impedance occurs at 1,15 KHz ($|Z_{s\min}| = 12\Omega$). At this same frequency, from Fig. 8, the impedance of the parallel converter is $|Z_p| = 0{,}05\Omega$. Thus, the relation between $|Z_{s\min}|$ and $|Z_p|$ is approximately 240. This is enough for the series converter to isolate the line from the load with respect to current harmonics of the load.

4 ACTIVE POWER FLOW THROUGH THE UPS SYSTEM

The direction of the active power flow through the UPS system is shown in Fig. 9. It can ever change because the amplitude of the input voltages is variable.

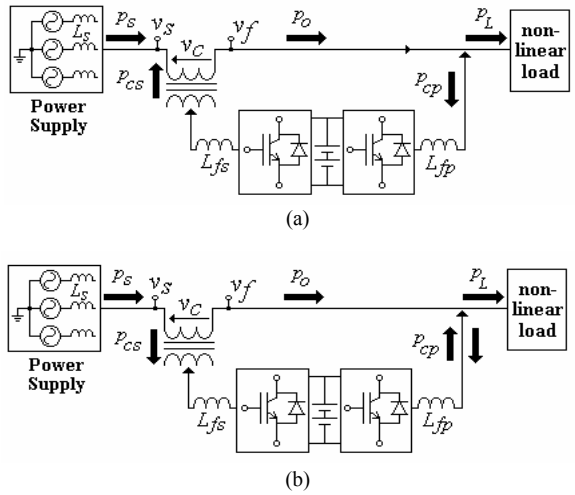


Figure 9. Power flow of the UPS system: (a) $V_s > V_f$; (b) $V_f > V_s$.

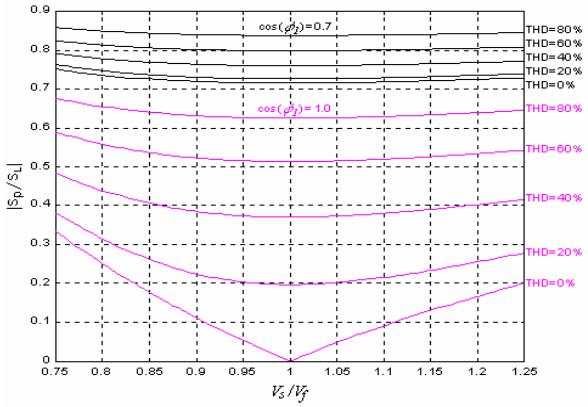
Both the apparent powers S_s and S_p, handled by the series and by the parallel converters, respectively, depend on the ratio between the output and input rms voltages (V_f / V_s), the displacement factor ($cos\,\phi_1$) and the THD of the load current i_L (THD_{iL}). In steady state, assuming a balanced sinusoidal system, the normalized powers handled by the parallel converter $|S_p/S_L|$ and by the series converter $|S_s/S_L|$ are given by equations (12) and (13), respectively. The quantities S_L, P_L, Q_L and H_L are the apparent, active, reactive and harmonic powers of the load, respectively.

In Fig. 10 (a) and (b) the normalized powers handled by the parallel converter $|S_p/S_L|$ and by the series converter $|S_s/S_L|$ are plotted for two different displacement factors ($cos\,\phi_1 = 1.0$ and $cos\,\phi_1 = 0.7$). These curves can be used to determine the power rate of the series and the parallel PWM converters.

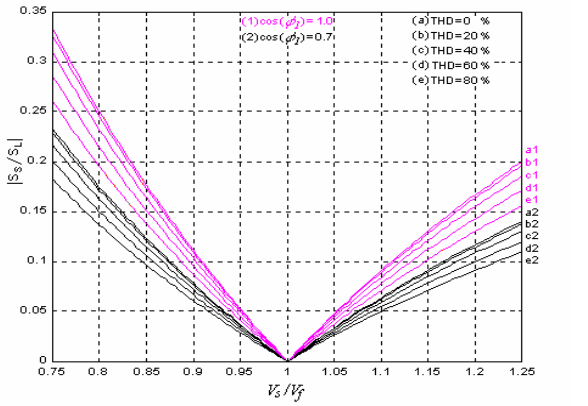
If the charging of the batteries is taking into account, additional active power P_b, given by (14), should be included in the analysis.

Thus, equations (16) and (17) replace equations (12) and (13), respectively, where the charging factor k_b is ever greater than zero, and P, given by equation (15), is the sum of active load power P_L and active power P_b, used to charge the battery bank.

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P_L^2\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P_L^2+Q_L^2+H_L^2}} = \frac{\cos\phi_1\sqrt{\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{1+THD_{iL}^2}} \qquad (12)$$



(a)



(b)

Figure 10. Normalized powers: (a) Parallel converter $|S_p/S_L|$, (b) Series converter $|S_s/S_L|$.

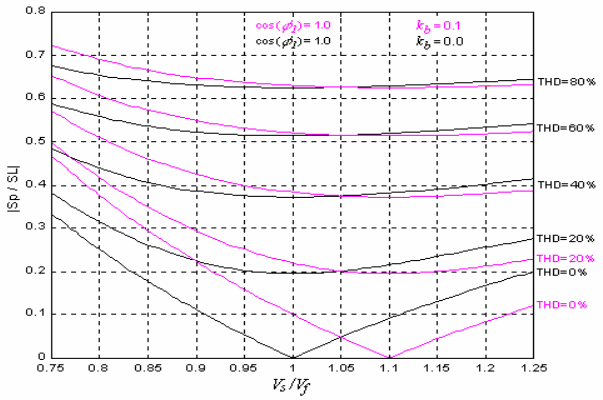
$$\left|\frac{S_p}{S_L}\right| = \sqrt{\frac{\cos^2\phi_1 \frac{V_f}{V_s}\left(\frac{V_f}{V_s}-2\right)}{1+THD_{iL}^2}+1} \quad (13)$$

$$P_b = k_b P_L \quad (14)$$

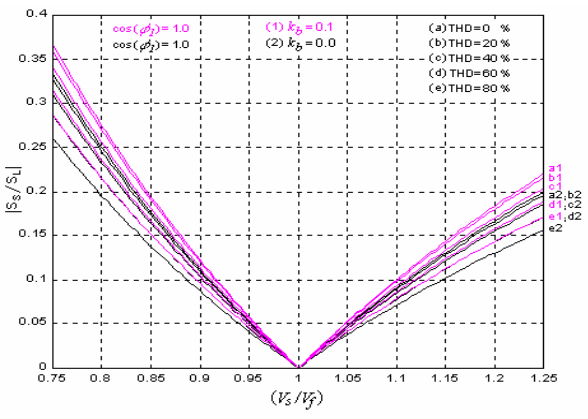
$$P = P_L + P_b = P_L(1+k_b) \quad (15)$$

$$\left|\frac{S_s}{S_L}\right| = \frac{\sqrt{P^2\left(1-\frac{V_f}{V_s}\right)^2}}{\sqrt{P_L^2+Q_L^2+H_L^2}} = \frac{\cos\phi_1\sqrt{\left[(1+k_b)\left(1-\frac{V_f}{V_s}\right)\right]^2}}{\sqrt{1+THD_{iL}^2}} \quad (16)$$

$$\left|\frac{S_p}{S_L}\right| = \sqrt{\frac{\cos^2\phi_1 \frac{V_f}{V_s}(1+k_b)\left(\frac{V_f}{V_s}(1+k_b)-2\right)}{1+THD_{iL}^2}+1} \quad (17)$$



(a)



(b)

Figure 11. Normalized Powers for $k_b = 0$ and $k_b = 0.1$ ($\cos\phi_1 = 1$):
(a) Parallel converter $|S_p/S_L|$,
(b) Series converter $|S_s/S_L|$.

The plots of the normalized powers for two different values of k_b ($k_b = 0$ and $k_b = 0.1$) are shown in Fig. 11 (a) and (b).

To fixed displacement factor ($cos\,\phi_1$) and load current THD, depending on the k_b value and the input voltage deviation from the desired output voltage, the batteries charging can be realized either from the series or parallel converters or from both as can be observed in Fig. 11 (a).

5 EXPERIMENTAL RESULTS

The complete scheme of the three-phase line-interactive UPS system is shown in Fig. 12. To verify the performance of the three-phase line-interactive UPS system, a prototype was developed and tested. Three single-phase non-linear loads with high load current THD are used to test the line interactive UPS system. The parameters used in the prototype are: L_{fp} = 300µH, L_{fs} = 1.4mH, C_{fp} = 130µF, R_{La} = 62 Ω, R_{Lb} = 55 Ω, R_{Lc} = 70Ω, $C_{L\,a,b,c}$ = 470µF, nominal rms line-to-neutral input voltages - $V_{s\,a,b,c}$ = 120V, nominal rms line-to-neutral output voltages - $V_{f\,a,b,c}$ = 115V and dc-bus voltage - V_{dc} = 570V. The apparent power rates of the unbalance loads are: S_a = 560 VA, S_b = 630 VA, and S_c = 540 VA.

The part of the scheme shown in the shaded area uses a 400MHz PC computer, a 12 bits resolution data acquisition system and a 12 bits resolution D/A converter board. Both current SRF controller and PLL system (Fig. 2) are implemented in software and are responsible to generate the current and voltage references for the current and voltage analog controllers. Both data acquisition systems and digital controllers run at 5kHz frequency.

The output voltages ($v_{f\,a,b,c}$) and load currents ($i_{L\,a,b,c}$) are shown in Fig. 13 (a), (b) and (c). Despite of the load current THD to be approximately 100% the THD of the regulated and balanced output voltages is less than 4%.

Fig. 14 (a) shows the three-phase source voltages $V_{s\,a,b,c}$ and Fig. 14 (b) shows the source currents $i_{s\,a,b,c}$. The parallel compensation currents ($i_{ca_p}, i_{cb_p}, i_{cc_p}$) are shown in Fig. 14 (c). It can be noted that the source currents are almost sinusoidal and balanced and their THD_{iL} are approximately 10%.

Details of the source currents, parallel compensation currents and uncompensated currents, for phases *a*, *b* and *c*, are shown in Fig. 15 (a), (b), and (c), respectively. Fig. 16

shows output voltage and input current of the phase *a*. Both input currents and output voltages are in phase with the input voltages. The measured power factor (*cos φ*) is equal to 0,982.

The neutral conductor load current and the neutral conductor utility current are shown in Fig. 17 (a) and (b), respectively. It is observed from Fig. 17 (b) that the amplitude of the utility neutral current has been reduced considerably.

The input voltage ($\boldsymbol{v_{sa}}$), the output voltage (v_{fa}) and the difference between them ($\boldsymbol{v_{ca}}$) are shown in Fig. 18 (a), which shows that the output voltages are in phase with respect the input voltages. For the load currents shown in Fig. 13 and the ratio between the output and input rms voltages (V_f / V_s) presented in Fig. 18 (a), the source reference currents $i^*_{sa,b,c} = i^*_{ca,b,c}$ obtained from the SRF-based controller of Fig. 2, can be seen in Fig. 18 (b).

The quantities v_{fa}, i_{sa}, i_{La} and i^*_{sa} (reference input current) are shown in Fig. 19 (a), for standby to backup transition mode that occurs at 0.02s. When the input power is out the input switch '*sw*' is opened and the input current i_{sa} drops to zero, but the output voltage v_{fa} remains providing power to the load. Thus, the PLL system forces the UPS to operate at a fixed reference frequency ($\omega^* =$ 377 rad/s).

The transition from backup to standby operation mode of the UPS system occurs at 0.31s, as shown in Fig. 19 (b) and (c). When the input power returns, the PLL system synchronizes the UPS system with respect the utility and the switch '*sw*' is closed. Thereby, immediately the input current i_{sa} follows the reference i^*_{sa}.

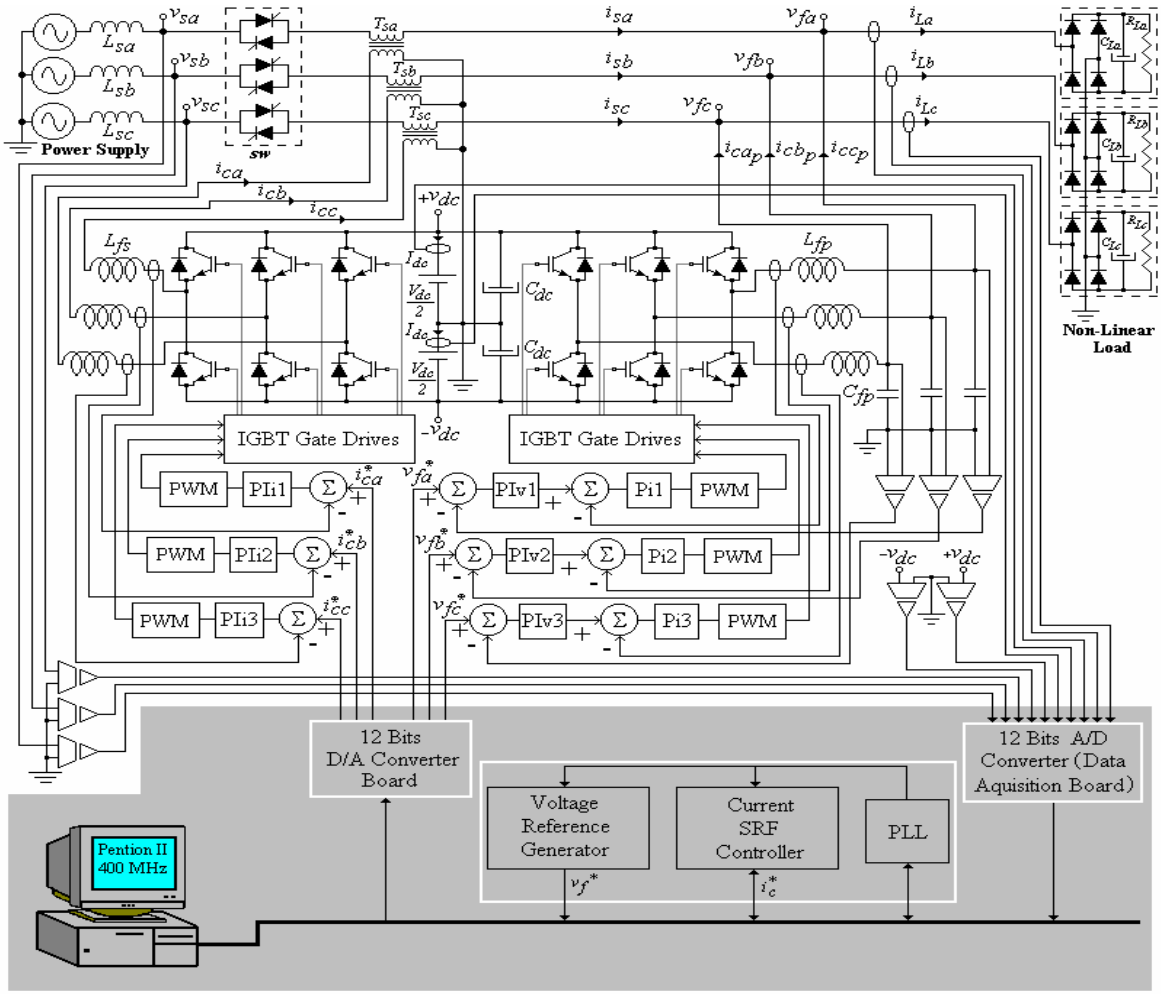
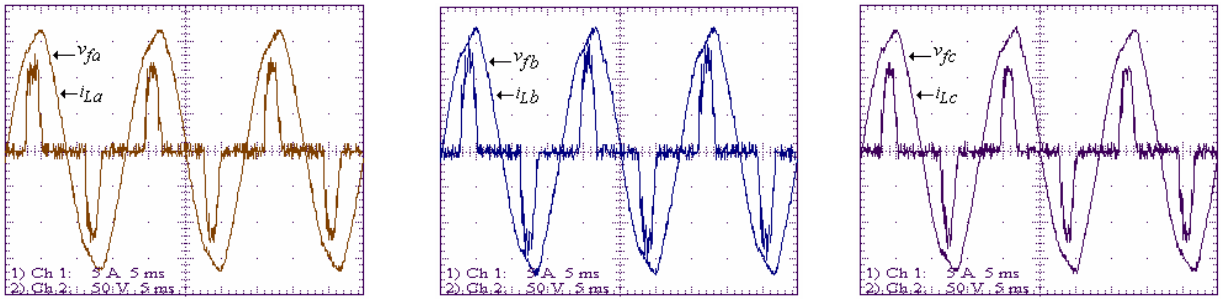
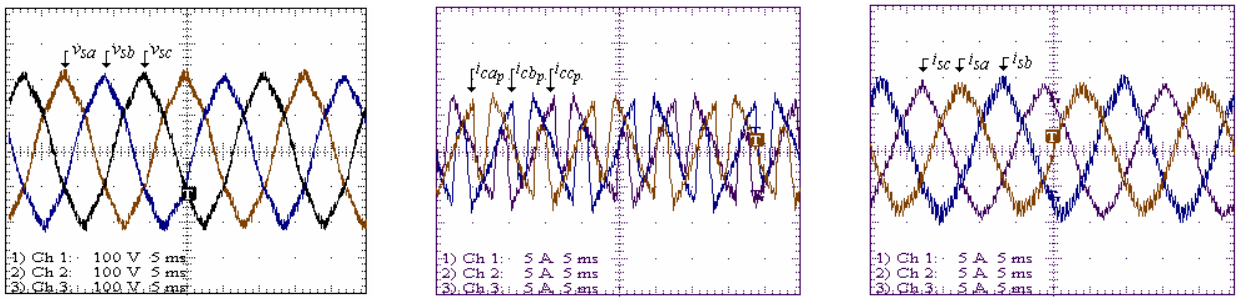


Figure 12. Complete scheme of the line-interactive series-parallel UPS system.



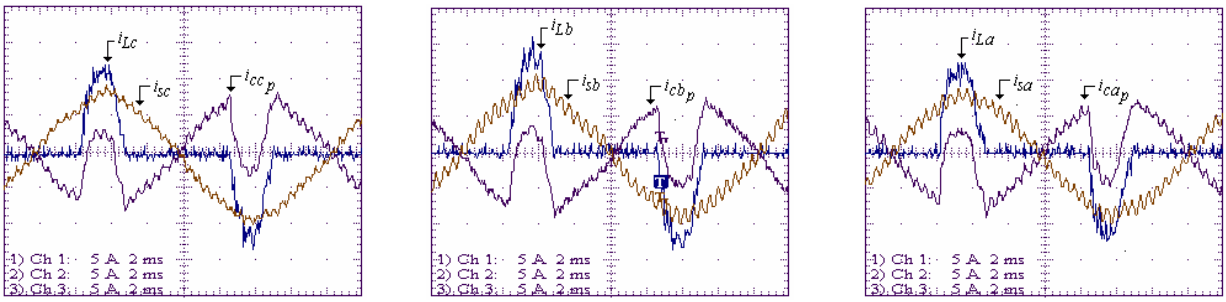
(a) (b) (c)

Figure 13. Output voltages (v_{fa} , v_{fb} , v_{fc}), and output currents (i_{La} , i_{Lb} , i_{Lc}): (a) Phase *a*; (b) Phase *b*; (c) Phase *c*.



(a) (b) (c)

Figure 14. (a) Input voltages (v_{sa} , v_{sb} , v_{sc}); (b) Input Currents (i_{sa} , i_{sb} , i_{sc}). (c) Parallel compensation currents (i_{ca_p} , i_{cb_p} , i_{cc_p}).



(a) (b) (c)

Figure 15. Details of the currents: (a) Phase *a* currents (i_{La} , i_{ca_p} , i_{sa}); (b) Phase *b* currents (i_{Lb} , i_{ca_p} , i_{sb}); (c) Phase *c* currents (i_{Lc} , i_{cc_p} , i_{sc}).

Note that the output voltage is unaffected by the transitions from standby to backup mode and from backup to standby mode. Fig. 19 (d) shows the UPS operating in standby mode.

Both Figs. 18 and 19 were obtained from data acquisition software.

6 CONCLUSIONS

A three-phase line-interactive UPS system topology with active series-parallel power-line conditioning capabilities has been implemented and tested for four-wire systems. With SRF-based controller implementation, balanced and almost sinusoidal input currents with low THD were obtained. The levels of both fundamental and harmonic contents of the utility neutral current have been reduced

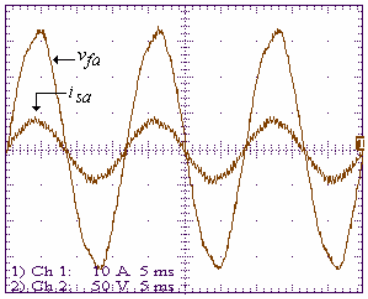
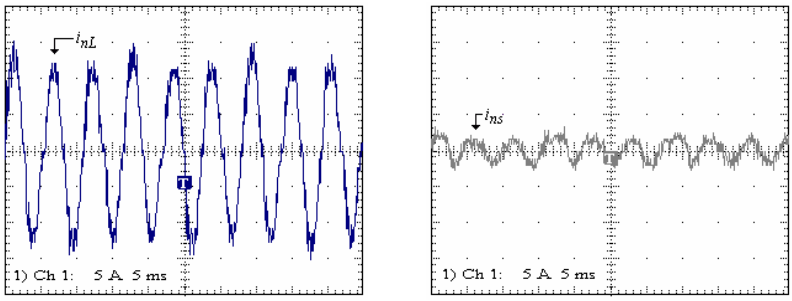
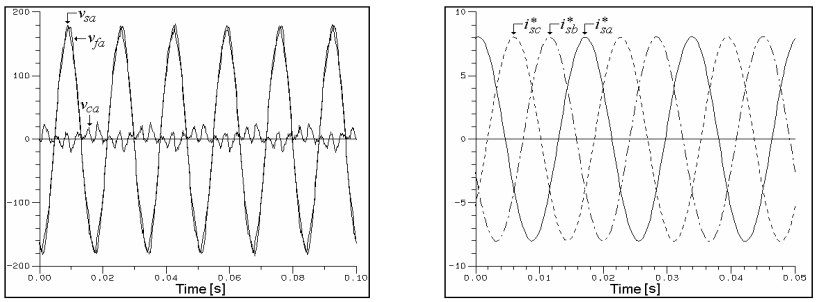


Figure 16. Phase *a* output voltage v_{fa}, and phase *a* input current i_{sa}.



(a) (b)

Figure 17. Neutral currents: (a) Load neutral current i_{nL}; (b) Utility neutral current i_{ns}.



(a) (b)

Figure 18. (a) Input voltage v_{sa}, output voltage v_{fa}, and compensation voltage v_{ca}; (b) Source reference currents (i^*_{sa}, i^*_{sb}, and i^*_{sc}).

considerably. The output voltages are balanced and almost sinusoidal with low THD.

The main advantage of the presented line-interactive UPS topology, when compared to the on-line topology, which uses two cascaded PWM power converters working at full power rating, is the smaller power rating handled by both series and parallel converters during the standby mode, increasing the efficiency of the UPS. The high series impedance and the low parallel impedance can protect the load against mains transients.

It has been demonstrated that the experimentally obtained results agree with good approximation with the theoretically predicted results.

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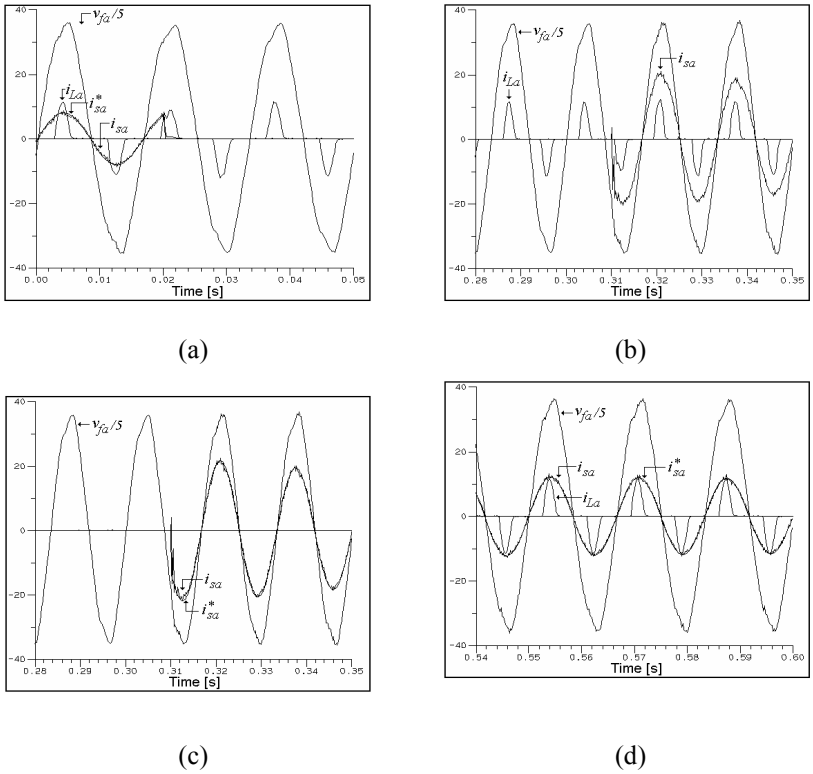

Figure 19. Transition modes: (a) Standby-Backup transition mode – output voltage v_{fa}, input current i_{sa}, reference input current i^*_{sa}, and output current i_{La}; (b) and (c) Backup-Standby transition mode; (d) Standby mode.

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