A NEW SIMPLIFIED SVPWM ALGORITHM BASED ON MODIFIED CARRIER SIGNAL

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RESUMO

Um novo algoritmo SVPWM simplificado baseado em sinal portador modificada

Este artigo apresenta um algoritmo simplificado da modulação por largura de pulso por vetores espaciais (SVPWM) para um inversor trifásico de dois níveis, o qual pode operar em submodulação e sobremodulação. Em outras simplificações achadas na literatura, as tensões de referência são modificadas e comparadas com um portador triangular para estimar os estados de comutação do inversor. Não obstante, este artigo propõe a modificação do portador, em lugar das referências. Este procedimento reduz o número de operações matemáticas e aumenta a velocidade de execução do algoritmo SVPWM em DSPs ou FPGAs. As ondas de referência são senoidais, ainda no modo de sobremodulação. Resultados de simulação e experimentais demonstram que a simplificação proposta produz o mesmo padrão de chaveamento que o SVPWM convencional, é mais simples e rápida que outras simplificações.

PALAVRAS-CHAVE: Inversor trifásico de dois níveis, modulação por largura de pulso por vetores espaciais, sinal portador triangular, submodulação, sobremodulação.

ABSTRACT

This paper presents a simplified algorithm of space vector pulse width modulation (SVPWM) for a two-level three-phase inverter, which can operate in undermodulation and overmodulation modes. In other simplifications founded in literature, the reference voltages are modified and compared with a triangular carrier to estimate the switching states of the inverter. However, this paper proposes the modification of the carrier signal instead of the references. This procedure reduces the number of mathematical operations and increases the execution speed of SVPWM algorithm in DSPs or FPGAs. The reference voltages are sinusoidal, even for overmodulation mode. Simulation and experimental results proves that the proposed simplification produces the same switching patterns than conventional SVPWM, is simpler and is faster than other simplifications.

KEYWORDS: Two-level three-phase inverter, space vector pulse width modulation, triangular carrier signal, undermodulation, overmodulation.

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1 INTRODUCTION

Space Vector PWM (SVPWM) is widely used in variable frequency drive applications, by its superior harmonic quality, less switching losses and extended linear range of operation (Holtz, 1994; Van der Broeck *e*t al., 1988; Yu *e*t al., 2008). However, its conventional implementation requires a high number of mathematical operations, reducing the maximum speed that SVPWM can be executed in DSPs or FPGAs.

Different researches were made to simplify SVPWM: The real and imaginary components of space vectors are used to calculate the switching times without using trigonometric functions (Shu *e*t al., 2007; Yu, 1999; Zhai and Li, 2008).

In Lamich *et* al. (2002), Zhang *et* al. (2009), the switching times are defined in terms of the phase references instead of using space vectors. According to Blasko (1997), Holmes (1996), SVPWM is equivalent to sinusoidal modulation when a zero-sequence component is added to the reference signals. In Pinheiro *et* al. (2005) SVPWM is easily implemented when the neutral points of the inverter and the load are connected, establishing the concepts of decomposition matrices.

On the other hand, the SVPWM algorithm must operate in overmodulation mode to generate as high AC voltages as possible for a given DC energy source. Different techniques in literature (Bakhshai *et* al., 2000; Filho *et* al., 2004; Pinto *et* al., 2000; Yang *et* al., 2009) modify the references signals, adapting the formulas for undermodulation mode to overmodulation mode. Those values are compared with a triangular carrier to establish the switching sequence.

In this paper, the number of mathematical operations to implement SVPWM algorithm, even for overmodulation mode, is reduced by the modification of the carrier signal instead of the references voltages.

The modified carrier depends on the zero-sequence component described in Blasko (1997) and the modulation index. On the other hand, the reference voltages are sinusoidal, even for overmodulation mode. This fact simplifies the implementation of SVPWM.

The proposed technique based on modified carrier is compared with conventional SVPWM, Hybrid PWM and the algorithm described in Filho *et*.al. (2004). Simulation and experimental results demonstrate that the proposed simplification based on modified carrier generates the same switching patterns than conventional SVPWM, requires a less number of arithmetic operations and its execution is faster than other simplifications.

2 SPACE VECTOR PWM

2.1 Two-Level Three-Phase Inverter

The structure of a two-level three-phase voltage source inverter is shown in Figure 1. It is composed by six power transistors (MOSFTET, IGBT, GTO) Q_a, Q_{an}, Q_b, Q_{bn}, Q_c and Q_{cn}, which are controlled by the digital signals s_a, s_{an}, s_b, s_{bn}, s_c and s_{cn}, respectively. To avoid short circuit in the energy source and indeterminate output voltages, the switching states of the upper transistors (Q_a, Q_b or Q_c) and the lower transistor (Q_{an}, Q_{bn} or Q_{cn} respectively) in the same leg are opposite.

Pole voltages v_{aN}, v_{bN} and v_{cN} are the terminal voltages of each leg respect to the neutral point N (reference point of the DC supply). These voltages depend of the switching states of the transistors (Yu, 1999), according to equation (1) :

$$v_{pN} = \begin{cases} 0,5v_{dc}; \text{if} s_p = 1(\text{switchedon}) \\ -0,5v_{dc}; \text{if} s_p = 0(\text{switchedoff}) \end{cases} \quad (1)$$

Where p denotes the phase of the inverter (p = a, b, c). Equation 1 indicates that each output of the inverter has two possible values. Therefore, there are 2^3 = 8 switching states, with their respective output voltages.

In general, the phase voltages (v_{aO}, v_{bO}, v_{cO}) of a balanced star-connected load fed by a three phase voltage source, as a two-level inverter, depend on the pole voltages (Bose, 2002):

$$\begin{bmatrix} v_{aO} \\ v_{bO} \\ v_{cO} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{bmatrix} \quad (2)$$

2.2 Space Vector Representation

A set of balanced three-phase voltages $[v_a v_b v_c]^T$ can be represented through a space vector, a complex number with a real (v_α) and an imaginary (v_β) components defined in the complex plane, according to equation (3) (Rashid, 2001):

$$\mathbf{V} = \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 2v_a - (v_b + v_c) \\ \sqrt{3}\,(v_b - v_c) \end{bmatrix} \quad (3)$$

Table 1 shows the space vectors that represents the eight switching states of the two-level inverter. Six non-zero vectors (from $\mathbf{V}_1$ to $\mathbf{V}_6$) divide the complex plane in six sectors of a hexagon, as illustrated in Figure 2. On the other hand, two zero vectors ($\mathbf{V}_0$ and $\mathbf{V}_7$) are located at the center of the hexagon.

Table 1: Output Voltages of the Two-Level Inverter

Vector	s_a	s_b	s_c	v_α	v_β
v_0	0	0	0	0	0
v_1	1	0	0	$-\frac{2}{3}v_{dc}$	0
v_2	1	1	0	$\frac{1}{3}v_{dc}$	$\frac{1}{3}v_{dc}$
v_3	0	1	0	$-\frac{1}{3}v_{dc}$	$\frac{1}{\sqrt{3}}v_{dc}$
v_4	0	1	1	$-\frac{2}{3}v_{dc}$	0
v_5	0	0	1	$-\frac{1}{3}v_{dc}$	$-\frac{1}{\sqrt{3}}v_{dc}$
v_6	1	0	1	$\frac{1}{3}v_{dc}$	$-\frac{1}{\sqrt{3}}v_{dc}$
v_7	1	1	1	0	0

The desired pole voltages $[v_{ra}v_{rb}v_{rc}]^T$ are represented by the vector $\mathbf{V}_r$, using equation (3) . According to equation (2) , if the pole references belong to a balanced system, then they are equal to the load phase references. This vector is approximated with a combination of the space vectors $\mathbf{V}_0$ to $\mathbf{V}_7$, during the modulation period t_m, according to equations (4) and (5) :

$$\mathbf{V_r}t_m = \mathbf{V_x}t_x + \mathbf{V_y}t_y \tag{4}$$

$$t_z = t_m - (t_x + t_y) \tag{5}$$

Where t_x, t_y and t_z are the switching times that $\mathbf{V}_x$, $\mathbf{V}_y$ and the zero vector $\mathbf{V}_z$ are used, respectively. If $\mathbf{V}_r$ is located in sector s: $\mathbf{V}_x = \mathbf{V}_s$ and $\mathbf{V}_y = \mathbf{V}_{s+1}$ (except in sector 6, where $\mathbf{V}_y = \mathbf{V}_1$).

Conventionally, the switching times are calculated using trigonometric functions, according to equations (6) and (7) (Bose, 2002):

$$t_x = \sqrt{3}t_m \frac{\|\mathbf{V_r}\|}{v_{dc}} \sin\left(\frac{\pi}{3} - g\right) \tag{6}$$

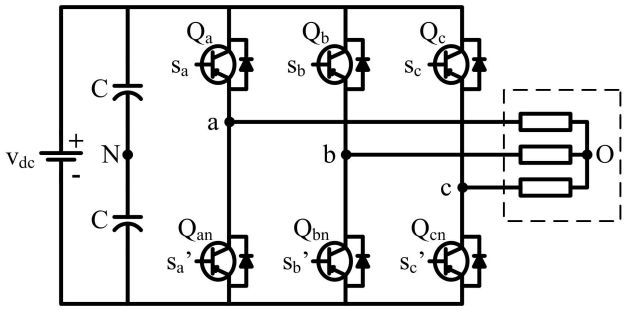

Figure 1: Two-level three-phase inverter.

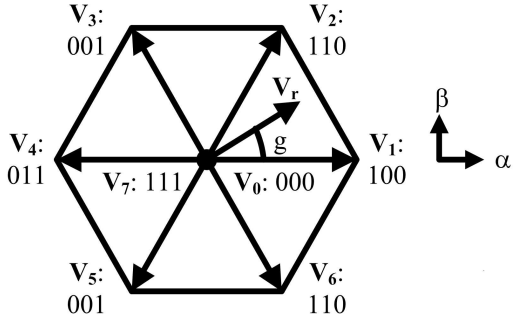

Figure 2: Zero and non-zero vectors of the inverter.

$$t_y = \sqrt{3}t_m \frac{\|\mathbf{V_r}\|}{v_{dc}} \sin(g) \tag{7}$$

Where $\| V_r \|$ is the magnitude of the reference vector, and g is the angle between $\mathbf{V}_r$ and $\mathbf{V}_x$, as shown in Figure 2. Trigonometric functions demand many mathematical operations in DSPs or FPGAs. In order to resolve this problem, the switching times can also be calculated using the real and imaginary components of the space vectors. Applying submatrix algebra (Cheng, 1999) to equation (4) :

$$\mathbf{V_r}t_m = \begin{bmatrix} \mathbf{V_x} & \mathbf{V_y} \end{bmatrix} \begin{bmatrix} t_x & t_y \end{bmatrix}^T \tag{8}$$

Figure 2 proves that the vectors $\mathbf{V}_x$ and $\mathbf{V}_y$ are not collinear. Therefore, the matrix $[\mathbf{V}_x\ \mathbf{V}_y]$ is invertible (Cheng, 1999). Considering $\mathbf{V}_r = [v_{r\alpha}\ v_{r\beta}]^T$, $V_x = [v_{x\alpha}v_{x\beta}]^T$ and $V_y = [v_{y\alpha}v_{y\beta}]^T$, the switching times can be calculated as follows:

$$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} \mathbf{V_x} & \mathbf{V_y} \end{bmatrix}^{-1} \mathbf{V_r} t_m$$
$$\begin{bmatrix} t_x \\ t_y \end{bmatrix} = \begin{bmatrix} v_{x\alpha} & v_{y\alpha} \\ v_{x\beta} & v_{y\beta} \end{bmatrix}^{-1} \begin{bmatrix} v_{r\alpha} \\ v_{r\beta} \end{bmatrix} t_m \tag{9}$$

Table 2 shows the values of t_x and t_y for each sector, according to equation (8) . The value of t_z is obtained using equation (5) . After those operations, the sequence of the switching states of the upper transistors must be defined. This arrangement can be done in different ways (Hariram and Marimuthu, 2005). This paper considers the software-determined switching pattern described in Yu (1999) and illustrated in Figure 3.

Table 2: Switching Times in Function of $v_{r\alpha}$ and $v_{r\beta}$

Sector	t_x	t_y
1	$\frac{t_m}{2v_{dc}}\left(3v_{r\alpha} - \sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{v_{dc}}\left(\sqrt{3}v_{r\beta}\right)$
2	$\frac{t_m}{2v_{dc}}\left(3v_{r\alpha} + \sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{2v_{dc}}\left(-3v_{r\alpha} + \sqrt{3}v_{r\beta}\right)$
3	$\frac{t_m}{v_{dc}}\left(\sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{2v_{dc}}\left(-3v_{r\alpha} - \sqrt{3}v_{r\beta}\right)$
4	$\frac{t_m}{2v_{dc}}\left(-3v_{r\alpha} + \sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{v_{dc}}\left(-\sqrt{3}v_{r\beta}\right)$
5	$\frac{t_m}{2v_{dc}}\left(-3v_{r\alpha} - \sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{2v_{dc}}\left(3v_{r\alpha} - \sqrt{3}v_{r\beta}\right)$
6	$\frac{t_m}{v_{dc}}\left(-\sqrt{3}v_{r\beta}\right)$	$\frac{t_m}{2v_{dc}}\left(3v_{r\alpha} + \sqrt{3}v_{r\beta}\right)$

2.3 Operation Modes of SVPWM

The modulation index m is defined as follows (Holtz, 1994):

$$m = \frac{\|\mathbf{V_r}\|}{\left(\frac{2}{\pi}v_{dc}\right)} \tag{10}$$

Where $2v_{dc}/\pi$ is the fundamental peak value of the square voltage wave. The modulation index varies from 0 to 1, defining three operation modes (Bose, 2002):

- Undermodulation mode ($0 \leq \ m <$ 0,907): The reference vector always reminds within the hexagon, while the reference voltages are perfectly sinusoidal.

- Overmodulation mode 1 (0,907 $\leq \ m <$ 0,952): The reference vector crosses the hexagon at two points in each sector. When SVPWM operates in overmodulation mode, there is a loss in the magnitude of the fundamental voltage. To compensate this effect, the reference voltages must be modified. In overmodulation mode 1, those references are composed by linear and sinusoidal segments.

- Overmodulation mode 2 (0,952 $\leq \ m \leq$ 1): The reference vector increases even further compared with overmodulation mode 1. The reference voltages are composed only by linear segments.

Figures 4, 5 and 6 show the operation region in sector 1 and the reference voltages for the three operation modes of SVPWM.

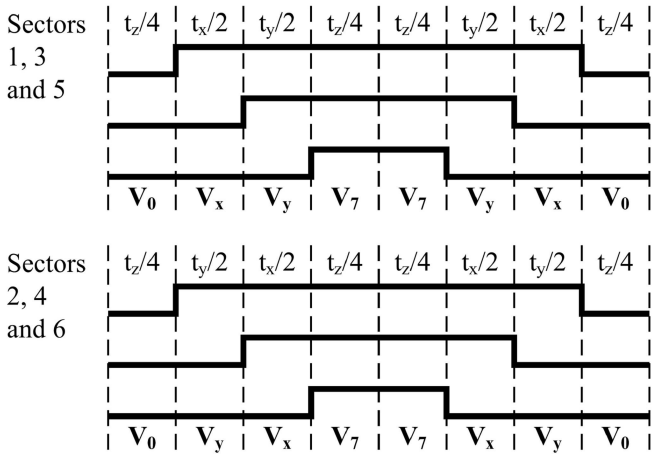

Figure 3: Software-determined switching sequence

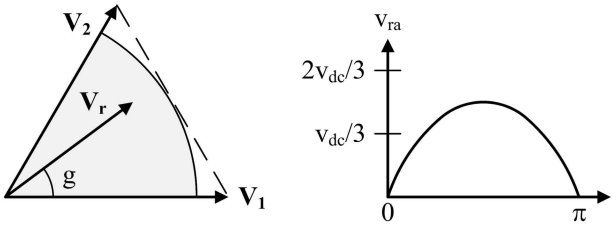

Figure 4: Operation region in sector 1 and reference voltage for undermodulation mode.

2.4 Turn-on Times

In order to simplify SVPWM algorithm, the turn-on times t_{a-on}, t_{b-on} and t_{c-on} are defined in Filho *et* al. (2004) to estimate the state of the upper transistors, to avoid working

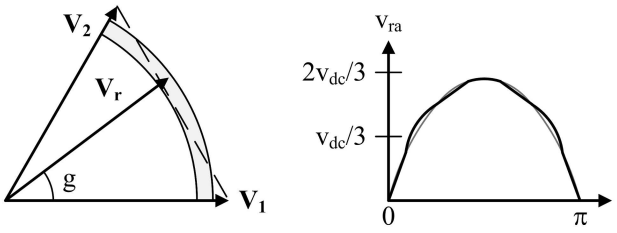

Figure 5: Operation region in sector 1 and reference voltage for overmodulation mode 1

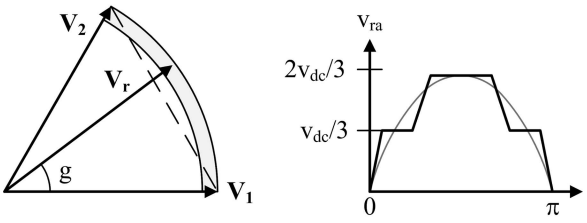

Figure 6: Operation region in sector 1 and reference voltage for overmodulation mode 2.

with the switching times t_x, t_y and t_z. The formulas of the turn-on times for the sector s (from 1 to 6) are presented in equations (11) , (12) and (13) :

$$t_{a-on} = \begin{cases} \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(-v_{r\alpha} - \frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(-2v_{r\alpha}\right)\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(-v_{r\alpha} + \frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 3,6 \end{cases} \tag{11}$$

$$t_{b-on} = \begin{cases} \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(v_{r\alpha} - \sqrt{3}v_{r\beta}\right)\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(-2\frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(v_{r\alpha} - \frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 3,6 \end{cases} \tag{12}$$

$$t_{c-on} = \begin{cases} \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(v_{r\alpha} + \frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(2\frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(v_{r\alpha} + \sqrt{3}v_{r\beta}\right)\right]; \mathrm{s} = 3,6 \end{cases} \tag{13}$$

The factor f_c compensates the attenuation of the fundamental voltage in overmodulation mode. This compensation factor can be implemented in a look-up table, and depends on the modulation index: f_c is unity in undermodulation mode, and it tends to infinite in overmodulation mode (Filho *et* al., 2004).

The advantages of working with turn-on times is that the switching states can be easily determined by a simple comparison with a triangular carrier $c(t)$, as illustrated in Figure 7 (Pinto *et* al., 2000). However, the formulas of the turn-on times require many mathematical operations for each sector and phase. This problem is solved using the concept of modified carrier signal, which is explained in sequence below.

3 PROPOSED ALGORITHM

3.1 Simplified Formulas about Turn-on Times

In Zhang *et* al. (2009), the switching times t_x and t_y are expressed in terms of the reference voltages. In this paper, the same strategy is used, but to express the turn-on times t_{a-on}, t_{b-on} and t_{c-on}. For example, according to equation (11) , the turn-on time for the phase a in sector 1 is:

$$t_{a-on} = \frac{t_m}{2}\left[1 + \frac{3f_c}{2v_{dc}}\left(-v_{r\alpha} - \frac{v_{r\beta}}{\sqrt{3}}\right)\right]; \mathrm{s} = 1,4 \quad (14)$$

On the other hand, based on equation (3) :

$$\begin{array}{l} -v_{r\alpha} - \frac{v_{r\beta}}{\sqrt{3}} = -\frac{2v_{ra}-(v_{rb}+v_{rc})}{3} - \frac{1}{\sqrt{3}}\frac{(v_{rb}-v_{rc})}{\sqrt{3}} \\ -v_{r\alpha} - \frac{v_{r\beta}}{\sqrt{3}} = \frac{-2(v_{ra}-v_{rc})}{3} \end{array} \quad (15)$$

As the sum of the three reference voltages is zero in a balanced three-phase system (v_{ra} + v_{rb} + v_{rc} = 0):

$$-v_{rc} = v_{ra} + v_{rb} \quad (16)$$

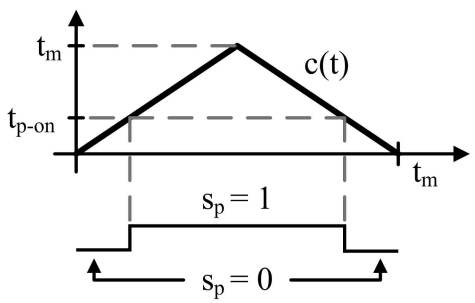

Figure 7: Comparison between t_{p-on} and the carrier c(t).

Replacing equations (15) and (16) in equation (14) :

$$\begin{array}{l} t_{a-on} = \frac{t_m}{2}\left[1 - f_c\frac{(v_{ra}-v_{rc})}{v_{dc}}\right]; \mathrm{s} = 1,4 \\ t_{a-on} = \frac{t_m}{2}\left[1 - f_c\frac{(2v_{ra}+v_{rb})}{v_{dc}}\right]; \mathrm{s} = 1,4 \end{array} \quad (17)$$

Using the similar procedure to obtain equation (17) , the turn-on times are defined in function of the reference voltages:

$$t_{a-on} = \begin{cases} \frac{t_m}{2}\left[1 - f_c\frac{(2v_{ra}+v_{rb})}{v_{dc}}\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{ra}+v_{ra})}{v_{dc}}\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{ra}+v_{rc})}{v_{dc}}\right]; \mathrm{s} = 3,6 \end{cases} \quad (18)$$

$$t_{b-on} = \begin{cases} \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rb}+v_{rb})}{v_{dc}}\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rb}+v_{ra})}{v_{dc}}\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rb}+v_{rc})}{v_{dc}}\right]; \mathrm{s} = 3,6 \end{cases} \quad (19)$$

$$t_{c-on} = \begin{cases} \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rc}+v_{rb})}{v_{dc}}\right]; \mathrm{s} = 1,4 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rc}+v_{ra})}{v_{dc}}\right]; \mathrm{s} = 2,5 \\ \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rc}+v_{rc})}{v_{dc}}\right]; \mathrm{s} = 3,6 \end{cases} \quad (20)$$

Equations (18) , (19) and (20) have the following structure:

$$t_{p-on} = \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rp} + v_{zs})}{v_{dc}}\right] \quad (21)$$

Where v_{rp} is the reference voltage in phase p, while v_{zs} is based on the zero-sequence component described in Blasko (1997), and depends on the sector s where the reference vector is located:

$$v_{zs} = \begin{cases} v_{rb}; \mathrm{s} = 1,4 \\ v_{ra}; \mathrm{s} = 2,5 \\ v_{rc}; \mathrm{s} = 3,6 \end{cases} \quad (22)$$

3.2 Modified Carrier Signal

Equation (21) can be expressed as follows:

$$t_{p-on} = \frac{t_m}{2} - f_c\left(\frac{t_m}{2v_{dc}}\right)(2v_{rp} + v_{zs}) \quad (23)$$

If the terms t_m/2 and t_m/($2v_{dc}$) are considered as constants, then six multiplications are needed to calculate the turn-on times using equation (23) , without considering the estimation of the compensation factor f_c.

However, it is possible to reduce even more the number of mathematical operations using the concept of modified carrier proposed in this paper.

Figure 7 indicates that the upper transistor Q_p is switched on (s_p = 1) when the carrier $c(t)$ is greater than the turn-on time:

$$c\left(t\right) \geq t_{p-on} \tag{24}$$

From equations (23) and (24) :

$$\begin{array}{l} c\left(t\right) \geq \frac{t_m}{2}\left[1 - f_c\frac{(2v_{rp}+v_{zs})}{v_{dc}}\right] \\ \frac{2c(t)}{t_m} \geq \left[1 - f_c\frac{(2v_{rp}+v_{zs})}{v_{dc}}\right] \\ 2v_{rp} + v_{zs} \geq \frac{v_{dc}}{f_c}\left[1 - \frac{2c(t)}{t_m}\right] \\ 2v_{rp} \geq \frac{v_{dc}}{f_c}\left[1 - \frac{2c(t)}{t_m}\right] - v_{zs} \end{array} \tag{25}$$

Dividing equation (25) by the amplitude of the reference vector $||V_r||$:

$$\begin{array}{l} \frac{2v_{rp}}{\|\mathbf{V_r}\|} \geq \frac{v_{dc}}{\|\mathbf{V_r}\|f_c}\left[1 - \frac{2c(t)}{t_m}\right] - \frac{v_{zs}}{\|\mathbf{V_r}\|} \\ \frac{2v_{rp}}{\|\mathbf{V_r}\|} \geq \left(\frac{2v_{dc}}{\|\mathbf{V_r}\|\pi}\right)\left(\frac{\pi}{2f_c}\right)\left[1 - \frac{2c(t)}{t_m}\right] - \frac{v_{zs}}{\|\mathbf{V_r}\|} \end{array} \tag{26}$$

By the definition of modulating index:

$$\frac{1}{m} = \frac{2v_{dc}}{\|\mathbf{V_r}\|\,\pi} \tag{27}$$

Replacing equation (27) in equation (26) :

$$\frac{2v_{rp}}{\|\mathbf{V_r}\|} \geq \frac{\pi}{2mf_c}\left[1 - \frac{2c\left(t\right)}{t_m}\right] - \frac{v_{zs}}{\|\mathbf{V_r}\|} \tag{28}$$

Four variables $v_{rp}n = v_{rp}/||\mathbf{V}_r||$, $v_{zsn} = v_{zs}/||\mathbf{V}_r||$, $k(t) = 1-[2c(t)/t_m]$ and $g(m) = \pi/(2mf_c)$ are defined as the normalized (from -1 to 1) reference voltage in phase p, the normalized zero-sequence component, a triangular carrier and a new correction factor, respectively. The waveforms of $g(m)$ and $k(t)$ are shown in Figures 8 and 9. Equation (28) can be expressed in function of these new four variables:

$$2v_{rpn} \geq g\left(m\right)k\left(t\right) - v_{zsn} \tag{29}$$

The modified carrier signal $q(t)$ is defined as follows:

$$q\left(t\right) = g\left(m\right)k\left(t\right) - v_{zsn} \tag{30}$$

The value of s_p (p denotes the phase a, b or c in the inverter) can be expressed in terms of the modified carrier $q(t)$:

$$s_p = \begin{cases} 1(\text{switchon}), \text{if} 2v_{rpn} \geq q\left(t\right) \\ 0(\text{switchoff}), \text{otherwise} \end{cases} \tag{31}$$

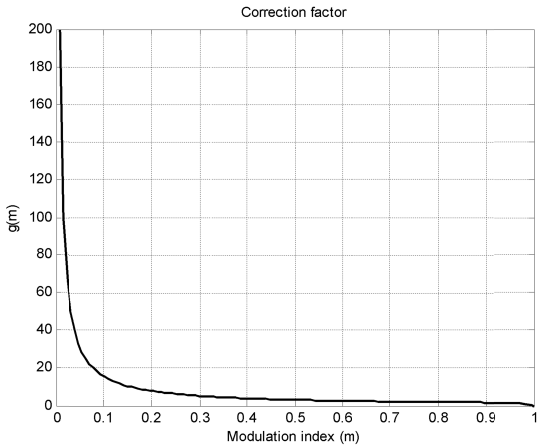

Figure 8: Correction factor g(m).

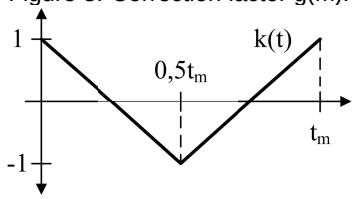

Figure 9: Normalized triangular wave k(t).

Sector identification is required to calculate v_{zsn} and $q(t)$. This problem is treated in the next section.

3.3 Sector Identification

In order to identify the sector and estimate the value of v_{zpn}, variables b_1, b_2, b_3, b_4 and b_5 are defined as follow:

$$b_1 = \begin{cases} 1; \text{if} v_{ran} \geq v_{rbn} \\ 0; \text{otherwise} \end{cases} \tag{32}$$

$$b_2 = \begin{cases} 1; \text{if} v_{rbn} \geq v_{rcn} \\ 0; \text{otherwise} \end{cases} \tag{33}$$

$$b_3 = \begin{cases} 1; \text{if} v_{rcn} \geq v_{ran} \\ 0; \text{otherwise} \end{cases} \tag{34}$$

$$b_4 = xor\left(b_1, b_2\right) \tag{35}$$

$$b_5 = xor\left(b_2, b_3\right) \tag{36}$$

Table 3: Sector Identification and Selection of v_{zsn}

Sector	Relation	b_1	b_2	b_3	b_4	b_5	v_{zsn}
1	$v_{rcn} < v_{rbn} < v_{ran}$	1	1	0	0	1	v_{rbn}
2	$v_{rcn} < v_{ran} < v_{rbn}$	0	1	0	1	1	v_{ran}
3	$v_{ran} < v_{rcn} < v_{rbn}$	0	1	1	1	0	v_{rcn}
4	$v_{ran} < v_{rbn} < v_{rcn}$	0	0	1	0	1	v_{rbn}
5	$v_{rbn} < v_{ran} < v_{rcn}$	1	0	1	1	1	v_{ran}
6	$v_{rbn} < v_{rcn} < v_{ran}$	1	0	0	1	0	v_{rcn}

Table 3 shows the values of these variables for the six sectors, calculated using the relations between the reference signals in each sector described in Zhang *e*t al. (2009). Equation (39) determines the value of v_{zsn}, based on Table 3 and the variables b_4 and b_5.

$$v_{zsn} = \begin{cases} v_{rbn}; \text{if} b_4 = 0 \text{and} b_5 = 1; \\ v_{ran}; \text{if} b_4 = 1 \text{and} b_5 = 1; \\ v_{rcn}; \text{otherwise}. \end{cases} \quad (37)$$

3.4 Complexity of the Proposed Simplification

Sector identification requires three comparisons (b_1, b_2, b_3), two XOR functions (b_4, b_5), two AND functions and two IF-THEN sentences. When v_{zsn} is known, the modified carrier $q(t)$ is calculated using only one multiplication, one subtraction and a look-up table. The terms $2v_{ran}$, $2v_{rbn}$ and $2v_{rcn}$ can be obtained by three additions, to avoid real-number multiplications.

As a result, the proposed simplification of SVPWM requires:

- Three additions;
- One subtraction;
- One multiplication;
- Two IF-THEN sentences;
- Three comparisons;
- Two XOR functions;
- Two AND functions;
- One look-up table for $g(m)$, with its respective operations.

One advantage of the proposed algorithm is that v_{ran}, v_{rbn} and v_{rcn} have unitary amplitude, independently of the modulation index. Only their frequencies change according to the desired electric frequency of the output voltages. Those signals are perfectly sinusoidal, even for overmodulation mode.

3.5 Comparison with other Modulation Techniques

The proposed technique is compared with the hybrid PWM (HPWM) and the simplification of SVPWM based on turn-on times, respect to their computational complexities (number of mathematical operations), to prove the advantages of the concept of modified carrier in the implementation of SVPWM.

Real-number arithmetic operations complicate the design and increase the execution time of the algorithms implemented in DSPs or FPGAs (Tzou and Hsu, 1997). Therefore, an algorithm with a less number of mathematical operations can be executed faster.

It is considered that the generation of the triangular waves, sinusoidal functions and look-up tables have the same computational complexity in all cases, while comparisons and Boolean operations are executed in a negligible time.

3.5.1 Comparison with HPWM

HPWM generates the same switching pattern of conventional SVPWM, using a triangle-comparison method (Blasko, 1997). In first place, the reference voltages with amplitude $||\mathbf{V}_r||$ and phase φ_p are produced through equation (40) :

$$v_{rp} = \|\mathbf{V_r}\| \sin(\varphi_p) \quad (38)$$

After that, the zero-sequence voltagev_{zh} is calculated:

$$v_{zh} = 0,5 \left[\min(v_{ra}, v_{rb}, v_{rc}) + \max(v_{ra}, v_{rb}, v_{rc})\right] \quad (39)$$

From Table 3 and equation (41) :

$$v_{zh} = 0,5 v_{zs} \quad (40)$$

The switching state in the phase p of the inverter is determined by the comparison established in equation (43) .

$$s_p = \begin{cases} 1(\text{switchedon}), \text{if} v_{rp} + v_{zh} \geq v_t(t) \\ 0(\text{switchedoff}), \text{otherwise} \end{cases} \quad (41)$$

According to Figure 9 and Blasko (1997):

$$v_t(t) = 0,5 v_{dc} k(t) \tag{42}$$

As HPWM does not operate in overmodulation mode, the comparison between this modulation technique and the proposed simplification of SVPWM will be made only for undermodulation mode, where f_c is unity (Filho *et* al., 2004) and $g(m)$ is calculated easily:

$$g(m) = \frac{\pi}{2m} \tag{43}$$

Replacing equations (42) , (44) and (45) in equation (30) , the upper transistors of the inverter are switched on (s_p = 1) in the proposed technique when the following inequality is satisfied:

$$\begin{array}{l} 2v_{rpn} \geq \frac{\pi}{2m} k(t) - v_{zsn} \\ 2v_{rpn} \geq \frac{v_{dc}}{\|\mathbf{V_r}\|} k(t) - v_{zsn} \\ \|\mathbf{V_r}\| v_{rpn} \geq 0,5 v_{dc} k(t) - 0,5 \|\mathbf{V_r}\| v_{zsn} \\ v_{rp} \geq v_t(t) - 0,5 v_{zs} \\ v_{rp} + v_{zs} \geq v_t(t) \end{array} \tag{44}$$

As a result, the switching states in the proposed simplification of SVPWM based on modified carrier signal are determined by equation (47) :

$$s_p = \begin{cases} 1(\text{switchedon}), \text{if} v_{rp} + v_{zh} \geq v_t(t) \\ 0(\text{switchedoff}), \text{otherwise} \end{cases} \tag{45}$$

Equations (43) and (47) are equal. Therefore, the proposed technique and HPWM produce the same switching pattern, both have a gain of 15% in the use of the DC-link voltage, their output voltages have the same harmonic distortion (THD) and dead times affect them in the same way.

The use of a look-up table requires many comparisons and mathematical operations. However, if the proposed technique will operate only in undermodulation mode, as HPWM does, the modified carrier is calculated from equations (32) and (45) :

$$q(t) = \frac{1}{m}\left[\frac{\pi}{2} k(t)\right] - v_{zsn} \tag{46}$$

Considering $r(t) = 0,5\pi k(t)$ as a new triangular carrier with the same computational complexity of $v_t(t)$ or $k(t)$, the proposed simplification can be implemented using three additions, one subtraction and one division. On the other hand,

Table 4: Number of Arithmetic Operations for HPWM

Procedure	Additions	Multiplications
Reference voltages	0	3
Estimation of v_{zh}	0	1
Addition of v_{zh} to the reference voltages	3	0
Total	3	4

Table 4 indicates that HPWM requires three additions and four multiplications. Equation (15) could be used in both algorithms to generate the third reference signal (for balanced three-phase systems). In that case, HPWM requires three multiplications. As a result, the proposed technique has less computational complexity than HPWM in undermodulation mode. It is only necessary a small one-dimensional look-up table to estimate $g(m)$ when overmodulation operation mode is needed.

3.5.2 Comparison with Other Simplifications of SVPWM

The proposed simplification based on modified carrier signal was deduced from the algorithm explained in Filho *et* al. (2004): Firstly, the turn-on times were expressed in terms of the reference voltages. In second place, the inequality that controls the switching states was expressed in terms of the modulation index and the zero-sequence voltage v_{zsn}. Finally, the modified carrier $q(t)$ was defined.

The main advantage of the proposed algorithm based on modified carrier signal, respect to other simplifications of SVPWM as the described in Filho *et* al. (2004), is that it requires a less number of mathematical operations because it works directly with pole references instead of space vectors. Equations (11) , (12) and (13) can be expressed as follows:

$$t_{p-on} = k_0 + f_c(k_1 v_{r\alpha} + k_2 v_{r\beta}) \tag{47}$$

Where k_0 = 0,5t_m, whilek_1 andk_2 depend of the sector and the phase. According to equation (**??**) , the calculus of the three turn-on times requires nine multiplications, six additions and two sinusoidal functions (to represent $v_{r\alpha}$ and $v_{r\beta}$).

On the other hand, equation (30) indicates the proposed simplification demands one multiplication, one subtraction and three additions. It is only necessary two sinusoidal waves for v_{ran} and v_{rbn}, because v_{rcn} can be obtained from equation (16) As a result, the proposed technique has less computational than the implementation of SVPWM using turn-on times.

4 RESULTS

4.1 Simulation Results

The proposed simplification of SVPWM was simulated in MATLAB/SIMULINK, as illustrated in Figure 10. The source voltage v_{dc} and the modulation period t_m were set in 200 V and 250 us (1/4 kHz), respectively.

The conventional SVPWM, HPWM and the algorithm described in Filho *e*t.al. (2004) were also simulated, as shown in Figure 11, in order to make comparisons with the proposed technique.

Three simulation tests were made, to cover undermodulation and overmodulation modes:

- Test 1 (Undermodulation mode): m = 0,85 ($||\mathbf{V}_r||$ = 108,23 V) and 60 Hz.;

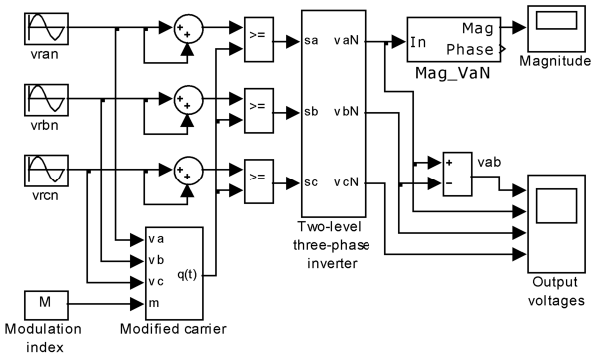

Figure 10: Simulation diagram of the proposed algorithm.

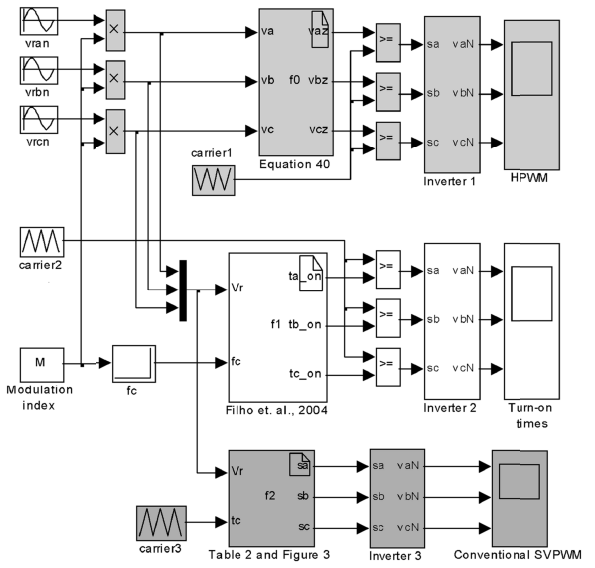

Figure 11: Simulation diagram for HPWM, conventional SVPWM and the simplification based on turn-on times.

Table 5: Peak Values of the Fundamental Components for the Simulation Tests.

Test	Reference (V)	Real (V)	Error (%)
1	108,23	108,18	0,042
2	119,68	119,57	0,095
3	124,78	124,78	-0,021

Table 6: THD of the Output Voltages for Test 1

Modulation technique	THD of pole voltage v_{aN}	THD of phase voltage v_{aO}
Conventional SVPWM	38,58%	22,76%
HPWM	38,58%	22,76%
Turn-on times	38,58%	22,76%
Proposed algorithm	38,58%	22,76%

- Test 2 (Overmodulation mode 1): m = 0,94 ($||\mathbf{V}_r||$ = 119,68 V) and 60 Hz;
- Test 3 (Overmodulation mode 2): m = 0,98 ($||\mathbf{V}_r||$ = 124,78 V) and 60 Hz.

The pole voltages and the line-to-line output voltages for the three tests are shown in Figures 12, 13 and 14. The magnitudes of the fundamental components of the pole voltages were founded using the Fourier Analyzer block of SIMULINK. The comparisons between the reference and the obtained pole voltages, presented in Table 6, prove that the proposed simplification can generate the desired voltages.

The total harmonic distortion (THD) of the pole voltage v_{aN} and the load phase voltage v_{aO} for the mentioned modulation techniques are shown in Tables 7 and 8. The load phase voltages were obtained through equation (2) , while THD was measured using the FFT Analysis Tool of MATLAB.

The proposed technique was compared in overmodulation mode only with the algorithm based on turn-on times because HPWM are not defined in this operation mode. The results indicate that the mentioned techniques have the same THD. Small differences in test 3 are produced by the numerical precision of the look-up tables.

Table 7: THD of the Output Voltages for Test 2 and 3

Modulation technique	THD of pole voltage v_{aN}	THD of phase voltage v_{aO}
Turn-on times: test 2	29,94%	16,41%
Proposed: test 2	29,94%	16,41%
Turn-on times: test 3	34,21%	17,35%
Proposed: test 3	34,19%	17,31%

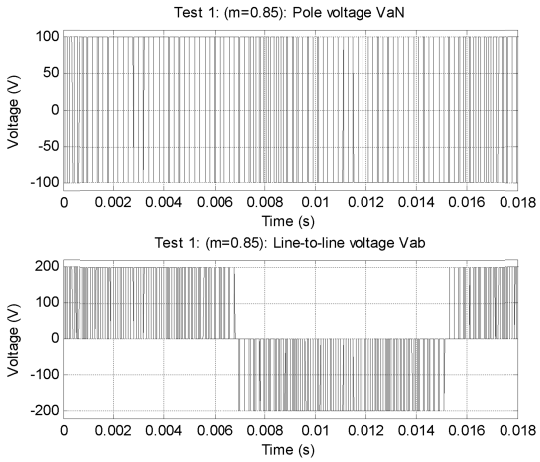

Figure 12: Test 1 (m = 0,85): Output voltages.

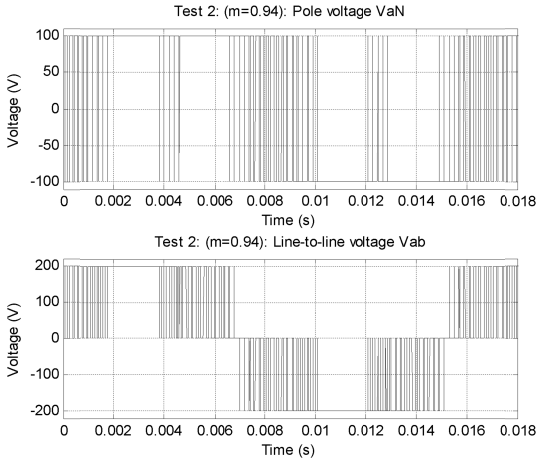

Figure 13: Test 2 (m = 0,94): Output voltages.

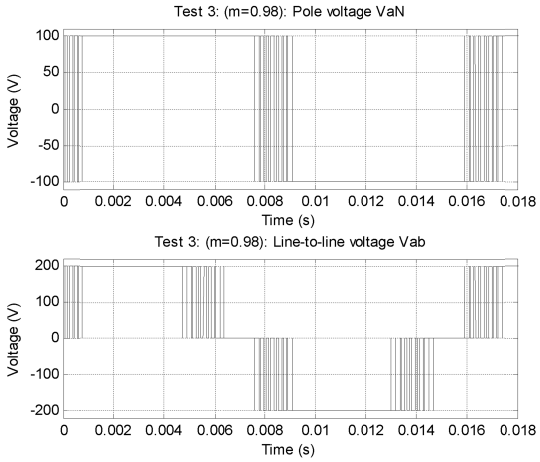

Figure 14: Test 3 (m = 0,98): Output voltages.

4.2 Experimental Results

The simplification of SVPWM based on the modified carrier signal was implemented in the DSP DSPACE DS1104, which is programmable using SIMULINK block diagrams.

The proposed simplification was applied in the open-loop speed control of an induction motor (3410 RPM, 60 Hz, 220 V_{rms}, 0,5 HP). The driver IRAMX16UP60A was used as the two-level three-phase inverter.

Three experimental tests were done using the same characteristics of the simulation tests. The line-to-line voltages shown in Figures 15, 16 and 17 are similar to the respective waveforms obtained in the simulation tests.

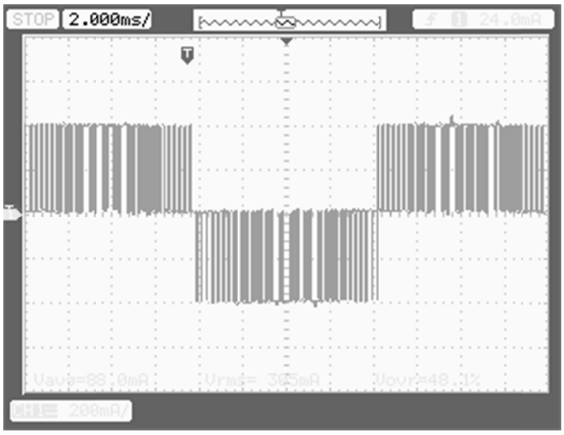

Figure 15: Test 1 (m = 0,85): Line-to-line voltage v_{ab}. Vertical scale: 100V/division.

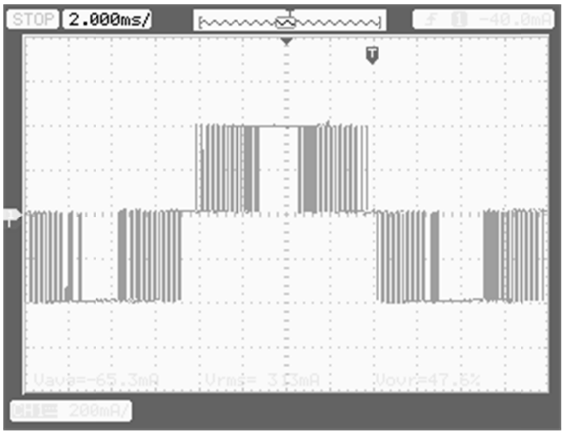

Figure 16: Test 2 (m = 0,94): Line-to-line voltage v_{ab}. Vertical scale: 100V/division.

Figures 18, 19 and 20 show the stator currents of the motor. An evident distortion in the waveform of the stator current appears in test 3, because the phase voltages which give en-

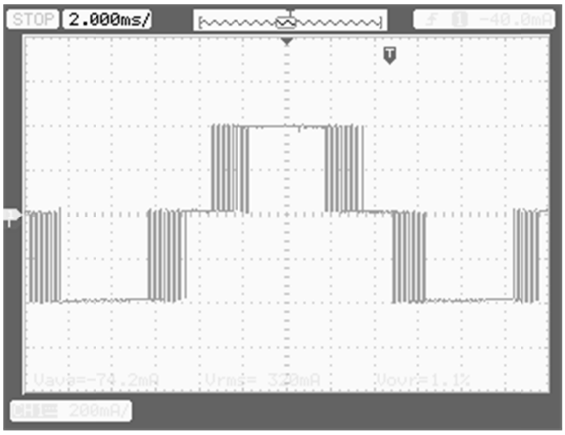

Figure 17: Test 3 (m = 0,98): Line-to-line voltage v_{ab}. Vertical scale: 100V/division.

ergy to the motor are near to the six-step operation (m = 1), where the harmonics of higher energy are concentrated in the low-frequency spectrum.

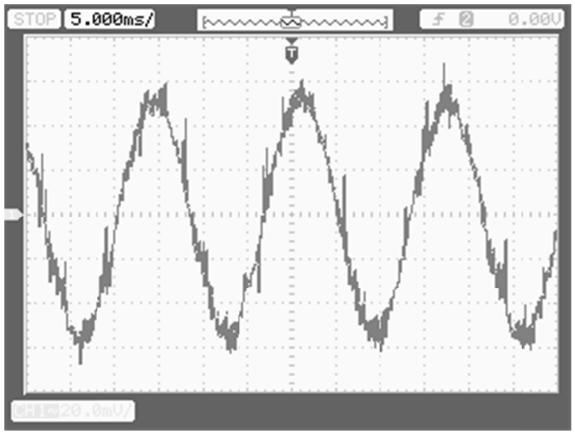

Figure 18: Test 1 (m = 0,85): Stator current i_a. Vertical scale: 200 mA/division.

4.3 Evaluation of Execution Time

The execution times of the proposed simplification and the algorithm presented in Filho *et* al. (2004) were compared experimentally. Both algorithms were designed in the files "proposed.mdl" and "reference.mdl" respectively. The SIMULINK diagram of the reference algorithm is presented in Figure 21. The MASTER-BIT-OUT blocks transfer the logic signals to the digital output ports of the DSP.

The time required in the execution of an algorithm determines the maximum sampling frequency ($f_s = 1/t_s$) that a DSP or FPGA can operate, because all the mathematical operations must be done before the beginning of the new sampling cycle. Otherwise, the algorithm can not be executed. Figure 22 illustrates this necessary condition.

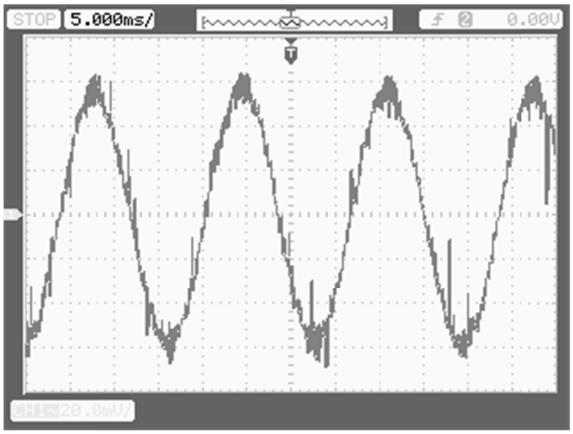

Figure 19: Test 2 (m = 0,94): Stator current i_a. Vertical scale: 200 mA/division.

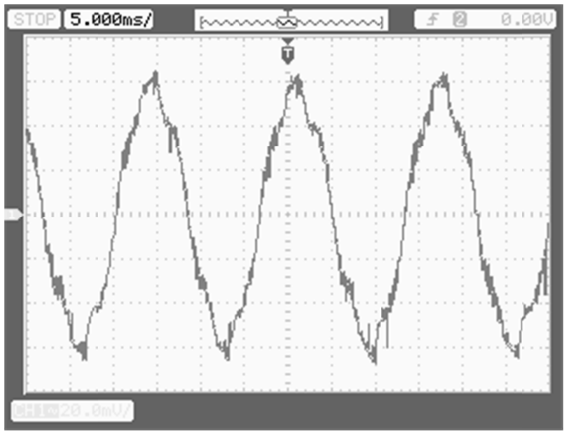

Figure 20: Test 3 (m = 0,98): Stator current i_a. Vertical scale: 200 mA/division.

Both algorithms were tested trying to be loaded in the DSP considering a sampling time of 12,5 us (1/80 kHz). Figures 23 and 24 present their respective loading processes. Only the proposed simplification was successfully loaded in the DSP. This fact proves that the proposed technique can be executed faster than the simplification described in Filho *et* al. (2004).

A simpler and faster SVPWM algorithm is suitable in the implementation of closed-loop variable frequency drive applications, because it allows working with higher sampling frequency to acquire information of currents, position or mechanical speed.

5 CONCLUSIONS

This paper presents a new simplification of SVPWM for undermodulation and overmodulation modes, based on the new

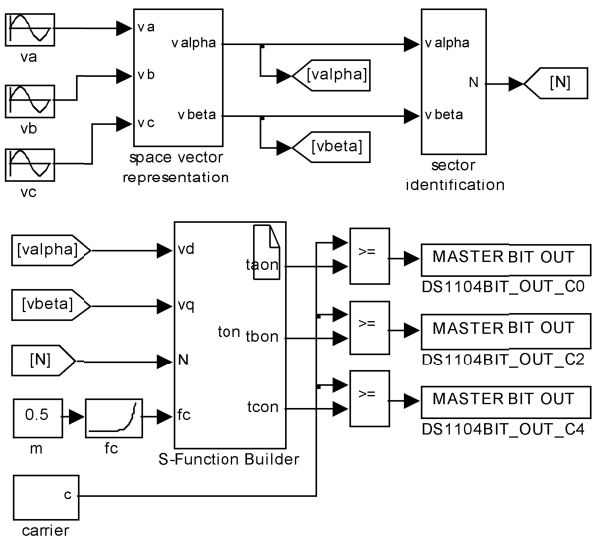

Figure 21: SIMULINK diagram of the SVPWM algorithm used as reference.

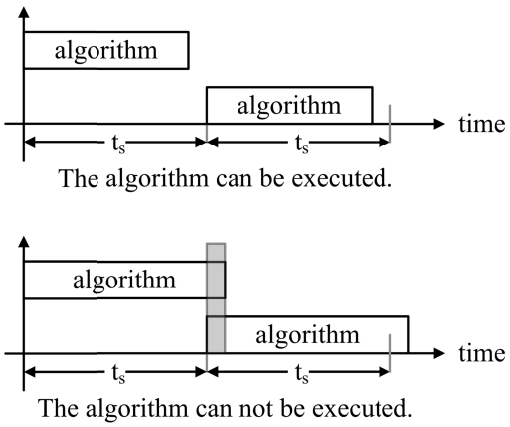

Figure 22: Requirement to execute successfully an algorithm in a DSP.

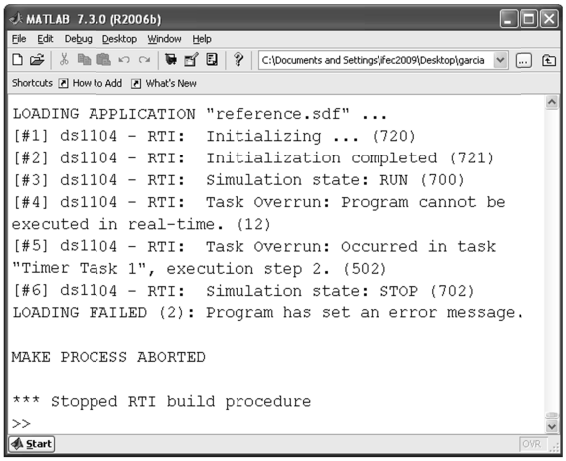

Figure 23: Loading process of the reference SVPWM simplification.

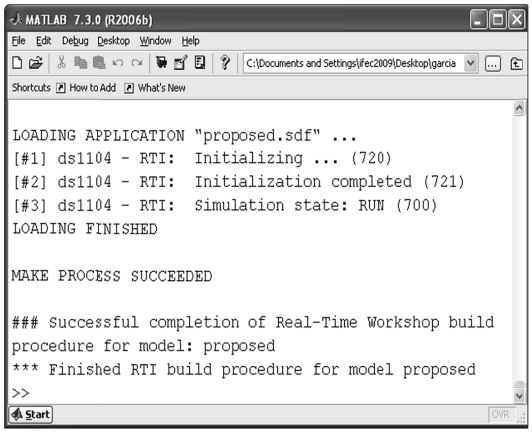

Figure 24: Loading process of the proposed SVPWM simplification.

concept of the modified carrier signal. This technique uses a small set of mathematical operations, while the sector identification is made using reference pole voltages and only requires a small one-dimensional look-up table to operate in overmodulation mode. The proposed simplification has a faster execution time in DSPs than other simplifications in literature, making possible the implementation of SVPWM algorithm in DSPs or FPGAs using higher sampling frequencies, which is suitable in variable frequency drive applications.

On the other hand, the proposed technique produces the same switching pattern that conventional SVPWM and HPWM. As a result, all these modulation technique produce the same harmonic distortion and are affected for dead times in the same way.

A future work consists in the use of the proposed simplification in a closed-loop speed control of three-phase motors.

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