AN ELECTRONIC SOLUTION FOR THE DIRECT CONNECTION OF A THREE-PHASE INDUCTION GENERATOR TO A SINGLE-PHASE FEEDER

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RESUMO

Este artigo propõe uma solução para a conexão direta de geradores de indução trifásicos em uma rede monofásica com regulação de vazão o que faz com que, a velocidade do gerador de indução se mantenha acima de sua velocidade síncrona. Para que a conexão entre gerador e rede monofásica seja satisfatória e para que os critérios de qualidade de energia sejam preservados, o controle do fluxo de energia, entre a rede monofásica e o conversor PWM trifásico, é realizado empregando a idéia de sistema interligado ajustando a defasagem e amplitude da tensão sintetizada pelo conversor em relação a tensão da rede monofásica de forma que o fator de potência na rede monofásica seja unitário. Em relação ao conversor de potência, espera-se que o mesmo produza tensões senoidais, com freqüência e amplitude fixas para que o gerador de indução opere balanceado. O artigo descreve a estratégia de controle do inversor, o critério de projeto dos controladores e apresenta alguns resultados experimentais.

PALAVRAS-CHAVE: Conversor PWM, Gerador de Indução, Controle Digital, Qualidade de Energia, Conversão Mono – Trifásica, Eletrificação Rural.

ABSTRACT

This paper proposes a solution for the direct connection of a three-phase induction generator to a single-phase feeder. This high power quality system is intended to be used in micro-hydro power plants applications with control of the water flow. It is employed to maintain the speed of the induction generator greater than its synchronous value. The difference between the generated power and the power consumed by the local load flows through the single-phase feeder. The power flow control is provided by a three-phase PWM in-

verter that additionally guarantees the local power quality. A system with good power quality must have sinusoidal and constant amplitude voltages, fixed frequency operation, balanced induction generator voltages and currents, harmonics and reactive power compensation. The paper describes the inverter control strategy, presents design criteria of the controllers, and shows experimental results.

KEYWORDS: PWM power converter, Asynchronous machine, digital control, power quality, single-phase to three-phase conversion, rural electrification.
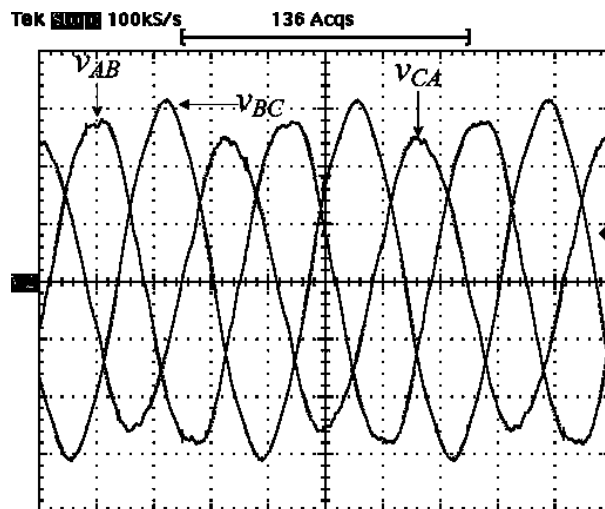
1 INTRODUCTION

The advantages of the three-phase induction machine have encouraged significant efforts in seeking approaches to overcome the Induction Generator (IG) poor voltage regulation and frequency variation (Simões and Farret, 2004; Marra and Pomílio, 2000). Some advantages of the induction machines are its robustness, simple construction, little maintenance requirements, wide availability, low cost, and higher power-weight ratio when compared with other electrical machines.

Customers in rural areas, that usually have a single-phase feeder, may request a three-phase system from the utility. However, it can be uneconomical with regard to the customers needed (Moncrief, 1996). On the other hand, there might be energy sources available in some of these areas to produce electric power. For this situation, some authors have proposed the direct connection of the induction generator to the single-phase feeder to obtain three-phase balanced voltages (Chan, 2007; Machado *et alii*, 1999). Some of these alternatives, based on the 'Steinmetz' connection, operate only under strict conditions and are affected by the AC load variations. An alternative technique is based on current control (Machado *et alii,* 1999), but this is not able to guarantee the AC voltage controllability.

2 PROPOSED SYSTEM

The proposed system comprises an IG directly connected to a single-phase feeder. As the direct connection of an IG to the single-phase feeder causes strongly unbalanced voltages and currents at the IG terminals as shown in Fig. 1, a three-phase inverter is connected to balance the IG voltages and, as a consequence, its currents.

Fig. 2 shows the complete system. The role of the Static Power Converter (SPC) is to regulate the power flow and to guarantee the local power quality. Such converter is a three-phase voltage source PWM inverter. The inductors L_{conv} are used to connect the inverter output to the Point of Common Coupling (PCC) where the IG, the local load and the single-phase feeder are connected. The AC capacitors (C_{conv}), to-

a)Voltages on the IG terminals (100 V/div).

Horizontal: 5 ms/div.
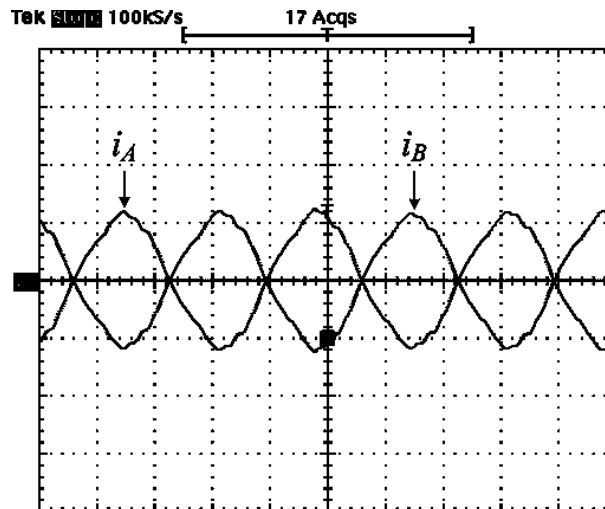
b) Currents on the IG terminals (10 A/div).

Horizontal: 5 ms/div.

Figure 1: Three-phase induction generator connected to the single-phase feeder.

gether with the inductors, provide the necessary high frequency filtering, resulting an AC voltage free of switching noise. Part of the total capacitance (C_{conv}) is designed to allow the IG self-excitation that could be necessary in case of islanding operation.

A characteristic of the proposed system is that it requires control on the water flow. The generated power depends on the prime-mover power availability. The power-flow control is based on the local load demand. If the local load demand is lower than the generated power, the excess is driven to the
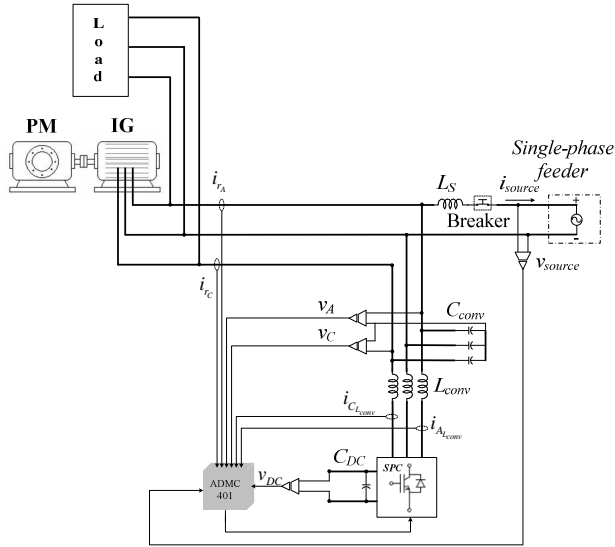
Figure 2: Proposed system structure.

feeder. Otherwise, it is possible to absorb additional power from the feeder.

If a contingence forces the system to go to islanding condition, i.e., to disconnect the feeder, and the local demand is higher than the generation, non-critical loads must be cut off. Otherwise, some strategy must be adopted to consume the excess of generated power as, for example, connecting additional loads in order to adequate the generated power to the demand. When the islanding operation must be concluded, it is necessary to guarantee the voltage synchronism before reconnecting the feeder.

Since the inverter does not manage real power, it is not necessary to have a DC source in the DC link. Nevertheless, as will be shown afterwards, the system is also able to the manage power provided by DC sources connected to the inverter DC side, as a battery bank or a photovoltaic panel.

3 SYSTEM OPERATION

The system operation imposes sinusoidal symmetric and balanced voltages on the AC bus. The stability of these voltages automatically provides the reactive power compensation, assuring that the IG will continue to run normally without losing magnetization, even feeding a heavy inductive load.

On the hypothesis that the inverter is able to maintain sinusoidal voltage for any kind of local load, and supposing the internal IG voltage and the feeder voltage are sinusoidal, their respective currents must also be sinusoidal. This means that the system also provides harmonic compensation, without any kind of current distortion measurement.

a) Delivering power to the feeder.
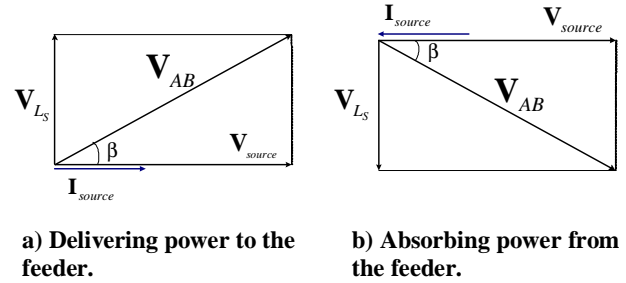
b) Absorbing power from the feeder.

Figure 3: Phasorial diagrams.

In fact, the filtering effectiveness depends on the inverter output impedance compared with the other system impedances (AC filter, IG and single-phase feeder impedances).

Another system feature is that the local voltage is adjusted in order to result in unity power factor (PF) to the single-phase feeder, maximizing the active power flow. The connection with such feeder is made with an inductor (L_S). In order to control the power flow, it is necessary to adjust the local AC bus voltage amplitude (V_{AB}) and the β angle between phasors V_{AB} and the single-phase feeder voltage (V_{source}). If the phasors I_{source} (single-phase feeder current) and V_{source} have the same direction the system delivers power to the feeder. Otherwise, if they have opposite directions, the system consumes power, as shown in Fig. 3.

To determine the β angle it is necessary to know the difference between the generated and the locally consumed power (P_r), the connection reactance (X_{L_S}) and to measure the rms voltage of the single-phase feeder (V_{source}) according to (1).

The voltage amplitude V_{AB} is calculated according to (2). Obviously, any variation on this voltage affects P_r. However, designing the coupling inductor for a small voltage drop, the variation in the AC local voltage can be small enough not to significantly affect the power calculation and the β angle. As the single-phase feeder voltage can vary, the local voltage has to follow such variation in order to maintain the unity power factor.

$$\beta = arctan\left(\frac{P_r X_{L_S}}{V_{source}^2}\right) \qquad (1)$$

$$V_{AB} = \frac{V_{source}}{cos\beta} \qquad (2)$$

3.1 L$_S$ Design criteria

The L_S design criteria takes into account the range of the single-phase feeder voltage variation. In a typical situation, as defined in (NE 08. CELPE, 1978; RER 03), the source
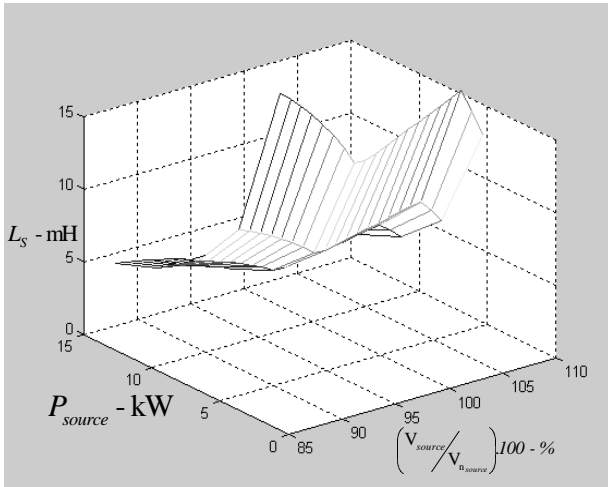
Figure 4: Coupling inductance value (L_S) for different power levels and PCC voltage.

voltage can vary from –7.5 % to +5 % around the rated value (Vn_{source}). In the worst case, the voltage variation can be –10 % to +5 %. As shown in Fig. 3, the voltage produced by the inverter must be higher than V_{source}. A 5 % increment is sufficient to allow a reasonable β angle resolution. Thus, the local voltage range is –5 % to +10 % around the rated value of the single-phase feeder voltage.

The inductance value can be determined considering that the rated power must flow through the feeder for any voltage in the given range. The induction value for voltage variation in different power levels can be found solving (3), and its result is shown in Fig. 4. Where ω_i is the fundamental frequency of the feeder in rad/s and the selected inductance must be the minimum value for a given power

$$L_S = \frac{tan(\beta)V_{source}^2}{\omega_i P_r} \quad (3)$$

3.2 Comparative efficiency between of the line-interactive and double conversion systems

The efficiency of the solution discussed in this paper can be compared to that of the conventional three-phase inverter + single-phase rectifier arrangement (double-conversion system).

It is important to underline that the percentage of load power flowing through the inverter stage of the proposed solution is always lower than unity, depending on the load configuration. Because of that, even if it was neglected the losses that, in a conventional double conversion solution, take place in

the rectifier stage, the proposed solution offers an efficiency improvement. To quantify that, it is possible to define a relationship between double-conversion and line-interactive efficiencies:

$$\eta_{double-conversion} = 1 - \frac{P_{losses\ double-conversion}}{P} = \eta_{conv} \quad (4)$$

$$\eta_{line-interactive} = 1 - \frac{P_{losses_{line-interactive}}}{P} \quad (5)$$

Now, if it was assumed the inverter stage has a given efficiency (η_{conv}), assumed to be constant for the two solutions, it can be said that:

$$P_{losses_{double-conversion}} = \frac{P_{losses_{line-interactive}}}{x} \quad (6)$$

where, P_{losses} represents the power lost in the inverter stage, P is the input power (assumed to be the same in both cases) and "x" is the percentage of input power that flows through the three-phase inverter in the line-interactive solution (depending on the load arrangement). In (6) basically is said that the power lost in the inverter stage is directly related to the power flowing through it, being the inherent inverter efficiency the same. This is a worst case assumption because, often, the converter processing lower power will have a higher efficiency. Nevertheless, substituting (6) into (4) and (5), the "efficiency gain" can be obtained as follows:

$$efficiency\ gain = \frac{\eta_{line-interactive}}{\eta_{double-conversion}} = x + \frac{1-x}{\eta_{conv}} \quad (7)$$

Fig. 5 represents the efficiency gain between the proposed solution (line-interactive system) and a double-conversion system. As can be seen, in all cases when the inverter of the line-interactive solution processes a fraction of the input power, there is an efficiency improvement, which can be particularly significant if the adopted inverter happens to have a relatively low inherent efficiency η_{conv}.

4 CONTROL STRATEGIES

4.1 Inverter Output Voltage Control

The inverter output voltage control system is a modified cascade scheme, with a fast inner current loop and an outer voltage loop. The system features, regarding power quality aspects, depend on its capability to maintain a regulated sinusoidal output voltage, independently of the load and power
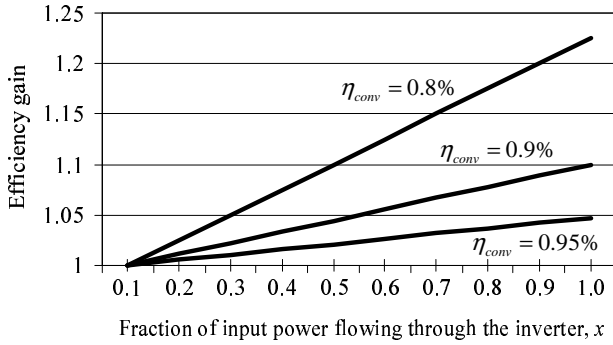
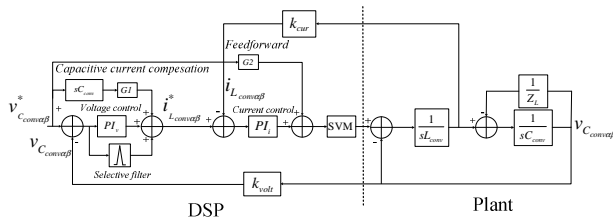Figure 5: Efficiency gain as a function of x and η_{conv}.

Figure 6: Overall model of the system.

flow conditions. This can be obtained since the inverter output impedance is substantially lower than the source and IG impedances. In this way, the inverter will be able to impose the three-phase voltage, as well as to conduct the greater part of the load current harmonics.

Such low output impedance is obtained not only by properly designing the output low-pass filter, but also using adequate control strategies. As shown in Fig. 6, selective filters are used to increase the gain at some selected frequencies in order to minimize the respective errors, thus improving the output voltage waveform quality (Buso *et alii*, 2001; Mattavelli, 2001). An additional feed-forward branch allows reducing the delay on the voltage correction due to the output filter capacitor. To have a faster response, the input of the space vector modulator block (SVM) receives a direct signal from the voltage reference.

The proportional-integral controller (PI) was chosen as the control technique. The current and voltage controls are implemented in the $\alpha\beta$ reference frame. The k_{cur} and k_{volt} gains represent the respective sensor scaling factors. The feed-forward gains G1 and G2 are always lower than one. The SVM block is the gain between space-vector routine and the output voltage produced by the inverter, including the inverter DC voltage value.

The desired closed loop cut-off frequency (ω_{CLi}) is 6.28 krad/s (1 kHz) and the respective phase margin (mf_i) is 70°. For these calculations the inverter output voltage is supposed

to be applied to a simple inductive load ($L_{conv} = 1.8$ mH), what is not exactly the case, but is an acceptable simplification. The uncontrolled system open loop gain (G_{OLi}) at the cut-off frequency, together with the performance parameters, defines the proportional and integral constants (k_{propi} and k_{inti}) according to (8) and (9) (Machado *et alii*, 2006; Machado *et alii*, 2005).

$$k_{propi}\frac{G_{OLi}}{\omega_{CLi}} = 1 \tag{8}$$

$$k_{inti} = k_{propi}\frac{\omega_{CLi}}{tan(mf_i)} \tag{9}$$

The closed loop cut-off frequency was chosen about one decade below the sampling frequency so that the current regulator still has a good compensation capability in the frequency range of interest.

Fig. 7a presents the closed loop frequency response of the current controller. Two situations are considered: the first one considers the load connected to the SPC terminals $Z_L = 0$ whereas, the other uses $Z_L = \infty$. There is a small error in the gain due to the output filter model simplification but it does not affect significantly the overall response. However the phase error is significant at the feeder frequency (60 Hz, 377 rd/s). A feed-forward of the voltage reference is used to guarantee a minimal error between current reference and the output current produced by the inverter.

The voltage loop guarantees a low error between the reference voltage, as calculated by (1) and (2), and the output voltages produced by the inverter. For the PI voltage compensator, the desired closed loop cut-off frequency (ω_{CLv}) is 628 rd/s (100 Hz) and the phase margin (mf_v) is 70°. These values, together with the system open loop gain (G_{OLv}), allow defining the proportional and integral constants k_{propv} (10) and k_{intv} (11).

$$k_{propv}\frac{G_{OLv}}{\omega_{CLv}} = 1 \tag{10}$$

$$k_{intv} = k_{propv}\frac{\omega_{CLv}}{tan(mf_v)} \tag{11}$$

Fig. 7b presents the closed loop response of the voltage PI showing a good agreement between no load ($Z_L = \infty$) situation and rated loading in the frequency range of interest.

Due the digital implementation and to the need for a reduced switching and sampling frequency (as required by the converter power rating) the voltage controller exhibits a low regulation bandwidth (a few hundred Hertz). To cope with that
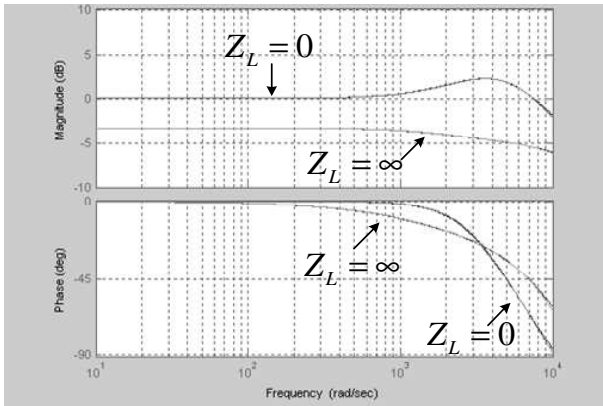
a) Close loop response of the current controller.
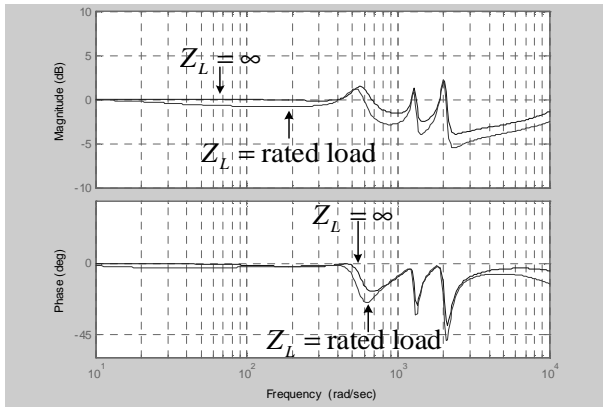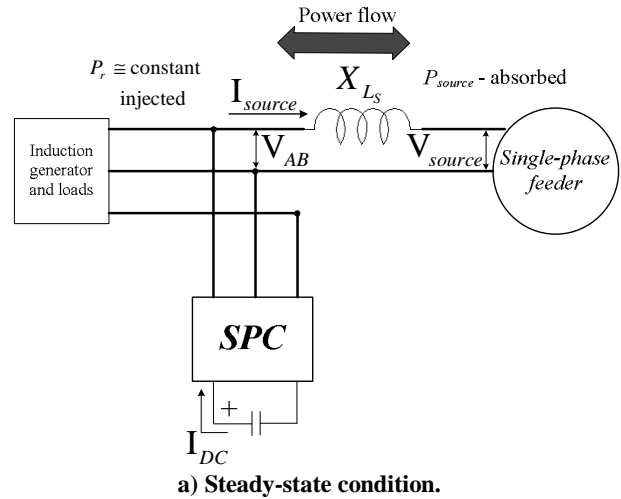

b) Close loop response of the voltage controller.

Figure 7: Bode diagram.

a) Steady-state condition.

b) Transient condition.

Figure 8: DC voltage correction.

and provide good control of the output voltage, a tuned resonant filter at the fundamental frequency, 3rd and 5th harmonics and a feed-forward of the capacitive current are put in parallel to the conventional voltage regulator, so as to boost the loop gain at the fundamental frequency. Thus, in the frequency range of interest both amplitude error and phase error are negligible, as can be seen in Fig. 7b (phase response) (Machado *et alii* , 2006; Machado *et alii*, 2005).
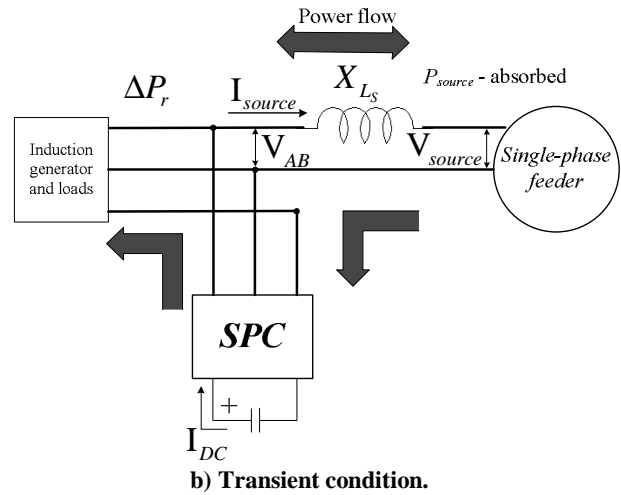
4.2 Inverter DC Link Voltage Control

When the power balance is disturbed due to: a load variation, a generated power fluctuation or to any single-phase feeder disturbance, the control system acts adjusting the voltage V_{AB} in order to alter the power flow in the single-phase feeder. During such transient, the power unbalance flows through the inverter, changing the DC voltage.

For example, in steady state the IG supplies the load and the remaining power is sent to the feeder. No active power flows

through the inverter. A sudden load increase will disturb such equilibrium until the new steady state pair (V_{AB}, β) is reached. The inverter provides the additional active power, consuming the energy stored in the DC link capacitor.

In order to maintain constant the DC bus voltage, the specific control circuit adjusts only the β angle, based on the DC link voltage deviation, as illustrated in Fig. 8. During the transient, the unity power factor restriction is relaxed; even so it is always close to unity.

For a perturbation in the DC voltage, while the new operation point is not established and considering the DC voltage is almost constant due to a high capacitance value.

$$\Delta P_r = \Delta P_{DC} = \Delta I_{DC} V_{DC} \qquad (12)$$

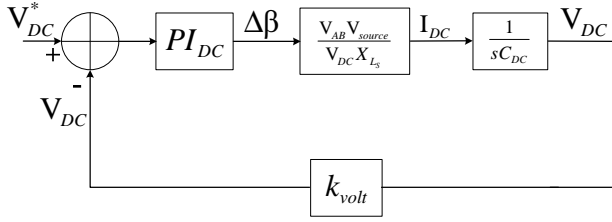For the compensation, the same power must be supplied for

Figure 9: DC link voltage control.

the single-phase source. The variation of P_{source} (ΔP_{source}) can be expressed as in (13). Assuming small β values, (13) can be linearized as in (14).

$$\Delta P_{source} = \frac{V_{AB}V_{source}}{X_{L_S}}sin\beta \qquad (13)$$

$$\Delta P_{source} = \frac{V_{AB}V_{source}}{X_{L_S}}\Delta\beta \qquad (14)$$

Substituting (14) into (12), the relation between a small β angle variation and the DC link current variation (ΔI_{DC}) can be found (15).

$$\Delta I_{DC} = \frac{V_{AB}V_{source}}{V_{DC}X_{L_S}}\Delta\beta \qquad (15)$$

Based on this model, it is possible to derive the block diagram of Fig. 9, which represents a linear approximation of the system that allows designing the DC link PI controller.

Similarly to the current and voltage control, the parameters for the PI controller are calculated for a closed loop crossover angular frequency (ω_{CLDC}) of 10.68 rad/s (1.7 Hz) and a phase margin (mf_{DC}) of 75°. For the open loop gain (G_{OLDC}) it is possible to calculate the proportional (16) and integral (17) constants k_{propDC} and k_{intDC}. The DC capacitance (C_{DC}) is 2820 μF and its design criterion can e found in Appendix A.
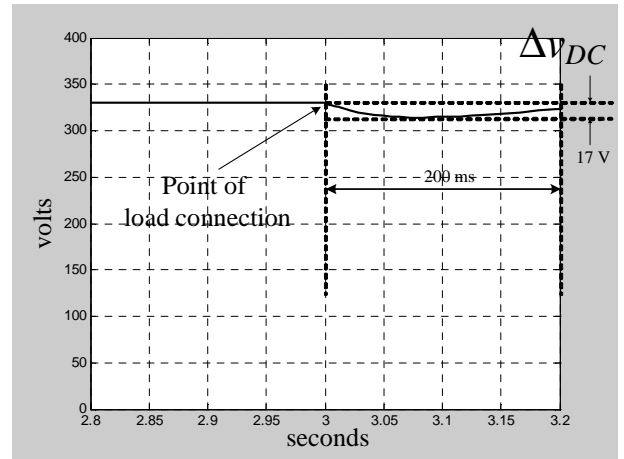
$$k_{propDC}\frac{G_{OLDC}}{\omega_{CLDC}} = 1 \qquad (16)$$

$$k_{intDC} = k_{propDC}\frac{\omega_{CLDC}}{tan(mf_{DC})} \qquad (17)$$

Figs. 10a and 10b represent a comparative dynamic response to experimentally verify the control algorithm presented in Fig. 9. Both tests take into account a 500 W single-phase resistive load step, imposed at the AC bus. As can be seen
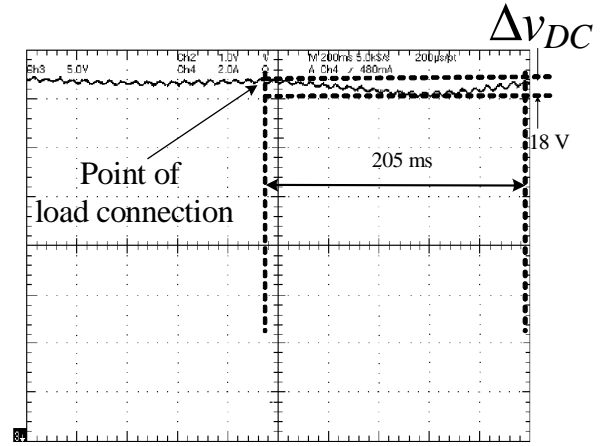
a) Vertical: 45 V/div. Horizontal: 40 ms/div (experimental result).

b) Vertical: 50 V/div. Horizontal: 50 ms/div (simulation result).

Figure 10: DC link voltage under load step.

the system behaves as expected, according to the design procedure. The simulated and measured time responses are very close ($\pm$ 200 ms each other) whereas the DC link voltage sag reaches 17 V (simulation) and 18 V (experimental), respectively.

5 EXPERIMENTAL RESULTS

The proposed control strategy has been implemented in the 16-bit fixed-point DSP ADMC 401. Space vector modulation was used to command the inverter at 12 kHz. This sampling frequency allows a resolution of 1.8 degrees for the output voltage synthesis. A 3 kW experimental setup was built to verify the system operation. The nominal parameters of the IG are found in presented in (Machado *et alii*, 2006; Machado *et alii*, 2005).

5.1 Steady-State Analysis

Fig. 11a presents two of the three-phase voltages produced by the inverter, after filtering. As desired, such voltages are balanced and the voltage displacement is around 120°. As expected, also the IG currents are also sinusoidal.

As a first test, the system feeds a balanced resistive load. Fig. 11b shows one inverter phase voltage (v_A) and the respective reference (v_A^*). The power that is not consumed by the load, P_r equal to 1800 W, is sent to the feeder. The inverter voltage THD is only 0.9 %. The PF between V_{source} and I_{source} is higher than 0.99. The local voltage THD is 2.2 % and the resulting current THD is 2.28 % respectively. Since the load voltage is sinusoidal, the feeder current will be distorted according to the voltage distortion and the coupling reactance.

As the feeder voltage is used to generate the internal references, the line voltage is filtered before the calculation of the inverter reference in order to avoid harmonic contamination.

Fig. 11c shows a situation in which the load power is higher than the IG power. The power deficit comes from the feeder. The feeder voltage leads the output inverter voltage, which results in the negative β angle. Also in this case the power factor is close to 1.
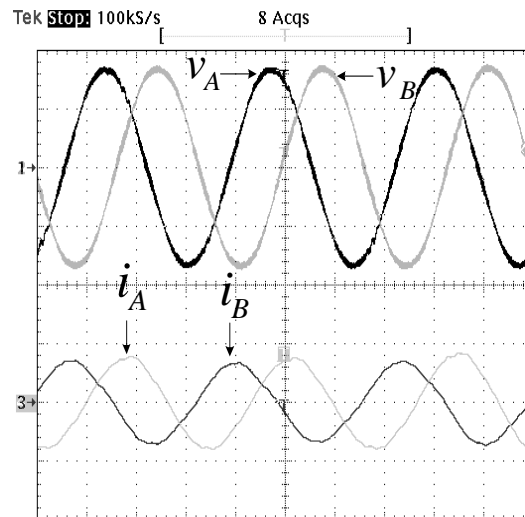
Fig. 11d shows the harmonic compensation provided by the inverter. The load is a 1200 W three-phase rectifier with capacitive filter (capacitance equal to 1mF). In spite of the non-linear load, both the IG and the feeder current are almost sinusoidal. The load and feeder current THD are, respectively 60 %, 6.8 %. The THD of the AC bus voltage is 3.2 % while the source voltage THD is 2.5 %.

5.2 Dynamic Analysis

Fig. 12 shows the system response to a single-phase load transient. The load is connected between B and C phases. At the connection, a very small reduction in the AC voltage takes place, according to the AC voltage control strategy, because it becomes necessary to absorb additional power from the feeder. Additionally, there is a DC link voltage sag, because that capacitor instantaneously has to deliver the additional power required by the load. As explained, the PI DC-link controller adjusts only the V_{AB} phase, so as the three-phase voltage amplitude is not affected due to the method employed to design the L_S.

6 CONCLUSIONS

This paper proposes a new strategy to compensate for the unbalanced operation of an induction generator connected to a single-phase feeder. A PWM inverter generates the con-


a) Voltages on the IG terminals (100 V/div) and respective currents (10 A/div) Horizontal: 5 ms/div.
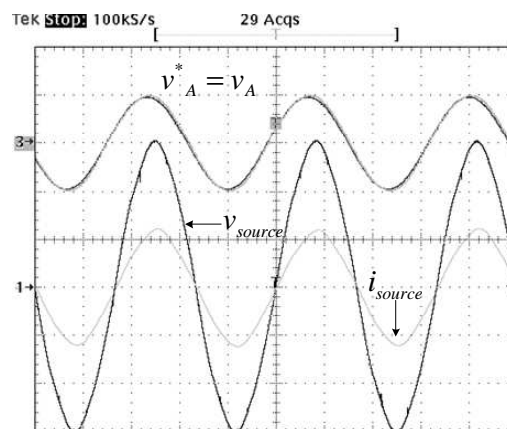
b) Top traces: reference and load voltage (180 V/div). Bottom traces: single-phase feeder voltage (100 V/div) and current (10 A/div). Horizontal: 5 ms/div.
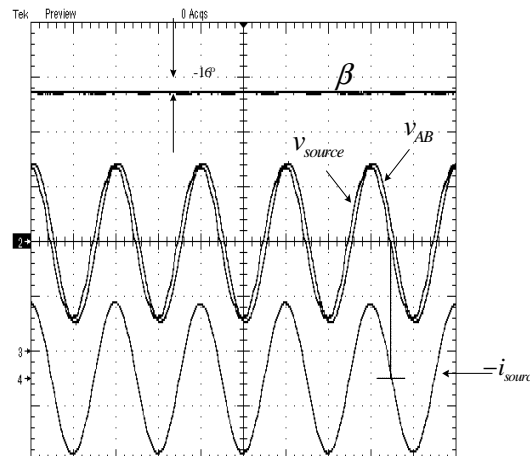
c) Top trace: angle β (500mV = 45°). Middle traces: AC bus and single-phase feeder voltage (180 V/div). Bottom trace: single-phase feeder current (10 A/div). Horizontal: 10 ms/div.
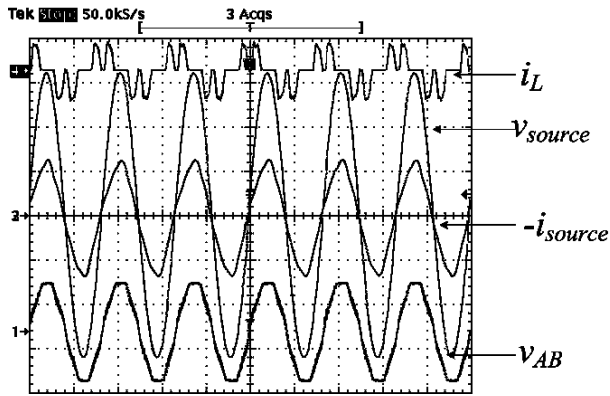
d) From top to bottom: load current (10 A/div), single-phase feeder voltage (100 V/div), current (10 A/div), and AC bus voltage (250 V/div). Horizontal: 10 ms/div.

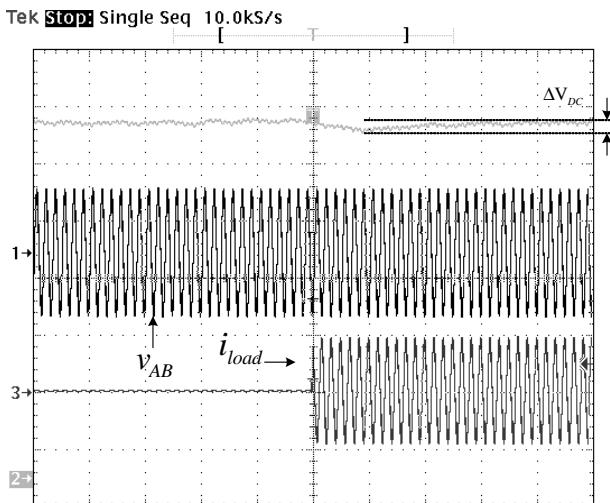Figure 11: Steady-state analysis.

Figure 12: Top trace: DC voltage (50 V/div). Middle trace: AC bus voltage (250 V/div). Bottom trace: load current (2 A/div). Horizontal: 50 ms/div.

trolled sinusoidal voltages necessary to equalize the IG currents and to control the single-phase feeder power flow.

By controlling the AC voltages phase and amplitude, it is possible to regulate the power flow through the single-phase feeder. If the locally generated power is higher than the load demand, the excess is delivered to the system. Otherwise, the power deficit is absorbed from the feeder. The system operation automatically compensates for load distortion, reactive power and unbalance, and guarantees low-distortion and unity displacement factor to the feeder current. The control system is implemented in a DSP, using PI regulators for both the inner current and the outer voltage loop. Additional feed-forward signals are used to improve the system dynamic response and power quality. The experimental results confirm the expectations.

ACKNOWLEDGMENT

APPENDIX A

To design the passive components of the step-up converter, it is necessary to consider at least the maximum current ripple ($\Delta I'_{DC}$), the double frequency of the fundamental (f_D), and DC bus voltage variation (18) (Machado *et alii*, 2006; McLandrich, 2003).

$$C_{DC} = \frac{\Delta I'_{DC}}{8 f_D \Delta V_{DC}} \qquad (18)$$

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