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Analysis of Total Ionizing Dose Effects on 0.13 μm Technology-Temperature-Compensated Voltage References

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ABSTRACT: The purpose of this work is to briefly discuss the effects of the total ionizing dose (TID) on MOS devices in order to estimate the results of future irradiation tests on temperature-compensated voltage references that are implemented on a mixed-signal chip fabricated using IBM 0.13 μm technology. The analysis will mainly focus on the effects of the parametric variations on different voltage references. Monte-Carlo analyses were performed in order to determine the effects of threshold voltage shifts in each transistor on the output voltage.

KEYWORDS: Ionizing dose, Radiation, TID, Voltage reference.

INTRODUCTION

Space and high-altitude aeronautical applications of electronics are exposed to a continuous action of ionizing radiation. The interaction between radiation and the structure of semiconductor devices results in undesired effects, which may be either transient or accumulated. Predicting these effects and accurately addressing solutions that guarantee operation under radiation is a challenge for the aerospace industry.

The transient effects occur when an energetic particle interacts with a sensitive region of the structure, resulting in a generation of charge that produces an electric pulse at a circuit node (Single Event Effect–SEE). Transient effects may result in hard errors, which are permanent, destructive, faults (Sexton, 2003); soft errors, which are non-destructive faults that affect circuit operation (Karnik and Hazucha, 2004); or disturbances that do not cause a fault.

Accumulated effects can be categorized into displacement damage (DD) and total ionizing dose effects (TID). Displacement damage occurs when the collision of a particle results in non-ionizing energy loss to the medium. This collision displaces an atom from the lattice, damages the crystalline structure of the silicon, and creates a defect that degrades electric parameters of the device (Srour, 2003). The TID usually result from accumulated charge in the dielectric and at the interface between the dielectric and the semiconductor, known, respectively, as oxide-trapped charge and interface-trapped charge.

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Ionizing radiation generates electron-hole pairs in the oxides of semiconductor devices. These electron-hole pairs suffer from an initial recombination that is a function of the electric field applied and the energy and type of the incident particle. After this initial recombination, the electrons, which have a higher mobility inside the insulator, escape from the oxide in a few picoseconds. The holes, on the other hand, have lower mobility and are eventually trapped in oxide traps, border traps or interface traps. The detailed mechanism of hole trapping in oxides can be found elsewhere (Oldham and McLean, 2003). In both NMOS and PMOS transistors, oxide-trapped charge is typically net positive, whereas interface-trapped charge is typically net positive for PMOS transistors and negative for NMOS transistors.

The consequence of this trapped charge is the degradation of electric parameters of the semiconductor devices, such as the threshold voltage, the leakage current, and the carrier mobility. It is also reported in the works of Fleetwood and Scofield (1990) and Fleetwood *et al.*, (1994) that TID effects increase the 1/f noise in MOS devices, as shown in Fig. 1. It should be noted that the spikes in Fig.1 are related to the power-line fundamental frequencies and their harmonics.

The 1/f noise in MOS devices is associated with charge carrier trapping near or at the interface between the semiconductor and the insulator. Charge trapping causes carrier number fluctuations and mobility fluctuations in the channel region of transistors. The activity of these traps results in discrete variations of the signal, known as Random Telegraph Signal (RTS), which, in MOS devices, is the major source of 1/f noise. It has also been reported that the annealing of the device after irradiation, for relatively thick oxides, results in a reduction of 1/f noise (Meisenheimer and Fleetwood, 1990), as observed in Fig. 2. The degradation of electric parameters of the device and the increase in the 1/f noise may either result in malfunction or fully disable an electronic system.

The purpose of this work is to review the TID effects on MOS devices in order to estimate the effects of an irradiation test on different temperature-compensated voltage references that are integrated in one chip using IBM 0.13 µm technology. Monte-Carlo analyses were performed in order to identify how parametric variations affect different topologies.

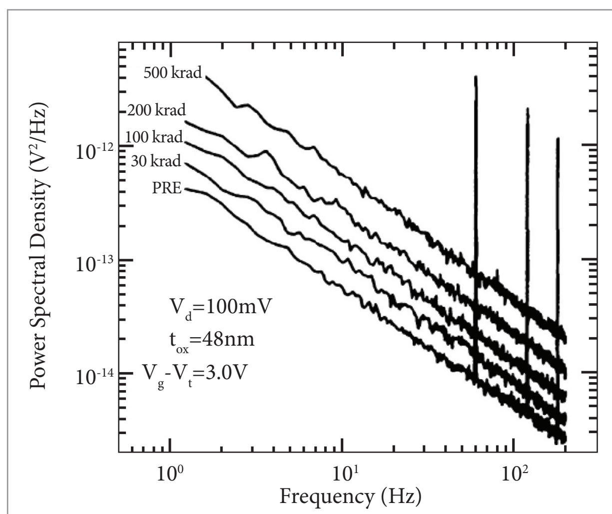

Figure 1. 1/f noise spectra for an irradiated NMOS transistor (oxide thickness of 48 nm). Adapted from Meisenheimer and Fleetwood, 1990.

TEMPERATURE-COMPENSATED VOLTAGE REFERENCES

Voltage references are building blocks that are present in a large variety of circuits; for instance, voltage regulators, comparators, and data converters. A voltage reference circuit should provide a stable output voltage despite variations in temperature, power supply, and process. Since voltage reference circuits can limit the accuracy of these applications, it is important to verify the impact of TID on the generated output voltage (V_{REF}).

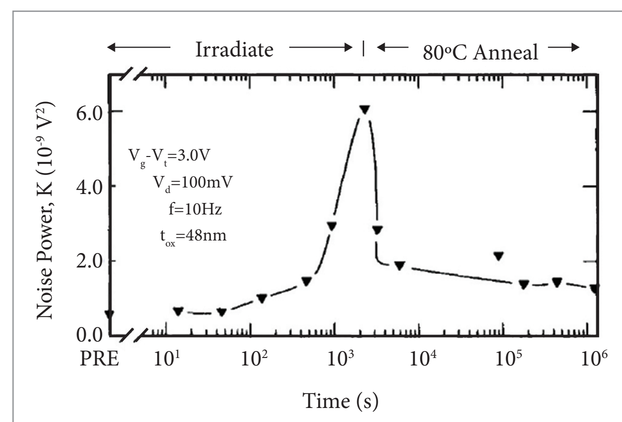

Figure 2. Noise power response during irradiation and annealing of an NMOS transistor (oxide thickness of 48 nm). Adapted from Meisenheimer and Fleetwood, 1990.

The traditional implementation for voltage reference is the bandgap circuit, where the generated V_{REF} is the bandgap voltage of silicon extrapolated to absolute zero Kelvin (i.e., ~1.2 V). Due to its stability regarding temperature and process, bandgap references have been used for the past forty years.

Bandgap references generate a temperature-compensated V_{REF} through a balanced sum of the diode voltage and the thermal voltage. The diode voltage (or base-emitter voltage) has a negative temperature coefficient (TC), while the thermal voltage has a positive TC. The thermal voltage is given by k*T/q, where k is the Boltzmann constant, T is the temperature and q is the electron charge.

Another topology of voltage reference that is widely used in the industry is the threshold-voltage-(V_{TH})-based reference. This topology of reference generates V_{REF} that is equal to the threshold of a transistor extrapolated to absolute zero Kelvin (Colombo *et al.*, 2011). The threshold-based voltage reference has gained increasing importance recently because of its ability to operate under low supply voltages (e.g., less than 1 V). Different from bandgap circuits that use diodes or BJTs, V_{TH}-based references use the gate-source voltage (V_{GS}) of MOS transistors to generate a voltage with negative a TC.

Bandgap and threshold-voltage-based references are two of the most frequently used techniques to generate temperature-compensated V_{REF} and, consequently, they are chosen as the case study for our project. An integrated circuit with five different voltage references was designed. In the fabricated chip, there are four references based on V_{TH}, shown in Figs. 3 to 5. and one bandgap-based reference, shown in Fig. 6.

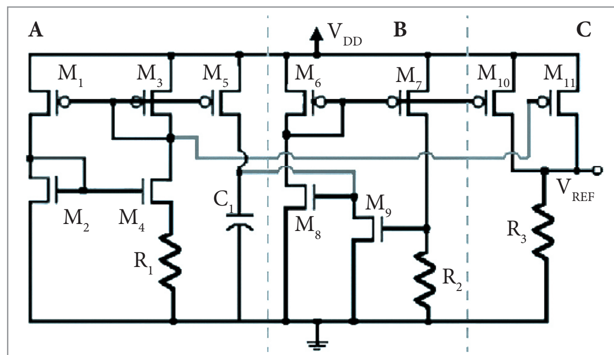

Figure 3. Simulated voltage reference 1 (Colombo *et al.*, 2011).

Reference 2 is the simplest V_{TH}-based voltage reference that can be implemented. Its output voltage is given by the sum of V_{GS} of M6 and the voltage across R2, which is proportional to the temperature. Reference 1 is similar to reference 2, but the temperature compensation is done by adding currents with opposite TC instead of voltages. Reference 3 and 4 are alternative V_{TH}-references that can be implemented with either one or none resistors, respectively. These architectures are appropriate for applications with requirement of a low silicon area. Reference 5 is a bandgap reference that uses a PMOSFET acting as a diode to generate V_{REF}. Further information regarding the designed voltage references can be found elsewhere (Colombo *et al.*, 2012; Banba *et al.*, 1999; Ueno *et al.*, 2009). These circuits were simulated under TID effects.

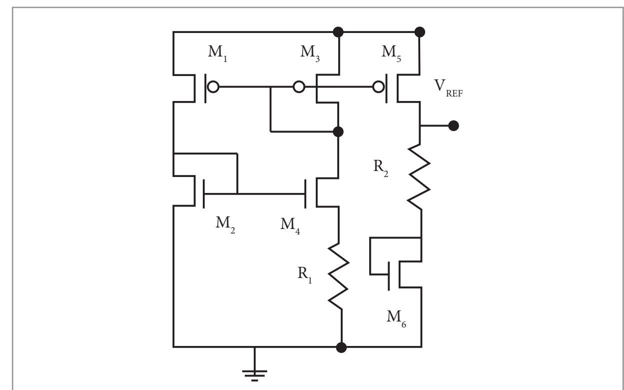

Figure 4. Simulated voltage reference 2 (Colombo *et al.*, 2011).

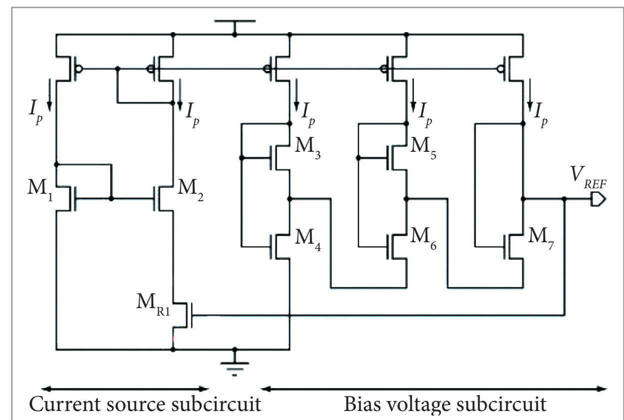

Figure 5. Simulated voltage reference 3 (using a resistor rather than the M_{R1} NMOS transistor) and voltage reference 4 (using the M_{R1} NMOS transistor) (Ueno *et al.*, 2009).

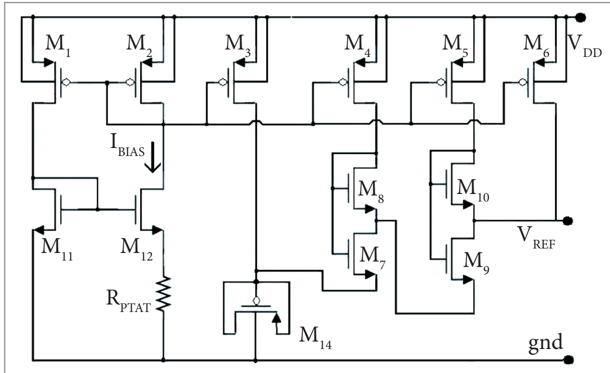

Figure 6. Simulated voltage reference 5 (Colombo *et al.*, 2012).

SIMULATIONS

In order to evaluate total ionizing dose effects on each voltage reference, SPICE simulations were performed, applying threshold voltage shifts to each transistor of the circuit. Data regarding threshold voltage shifts due to total ionizing dose effects on 0.13 µm MOS transistors were obtained from (Haugerud *et al.*, 2005).

The voltage references were simulated for different bias conditions and under different temperature conditions. A total of 10,000 Monte-Carlo simulations were performed for each voltage reference. Process variability, provided in the IBM 0.13 µm commercial design kit, was also included in thesimulations, in an attempt to evaluate TID effects for different circuit conditions. For each of the 10,000 Monte-Carlo simulations, threshold voltage shifts due to process variability and also due to total ionizing dose effects were pseudo-randomly selected from normal distributions and assigned to each transistor of the circuit, meaning that for each simulation every transistor has its own threshold voltage shifts due to TID and also due to variability. It is important to state that data regarding total ionizing dose effects on 0.13 µm technology obtained from (Haugerud, *et al.*, 2005) were not obtained for the 0.13 µm IBM technology used for integration and simulation.

For references 1, 2, 3, and 4, DC simulations were performed for temperature conditions ranging from -40°C to 80°C, at a fixed supply voltage of 1.2 V. For reference 5, DC simulations were performed for temperature conditions ranging from -40 to 80°C, at a fixed supply voltage of 2.5 V. All simulations were performed while considering a pre-irradiation situation (0 krad) and under total doses of 50 krad (Si) and 70 krad (Si).

RESULTS AND DISCUSSION

The output voltage obtained for the five voltage references simulated under 0 krad (Si), 50 krad (Si), and 70 krad (Si) is presented in Figs. 7 to 11. The variation of the standard deviation as a function of temperature and total dose is presented in Tables 1 to 3.

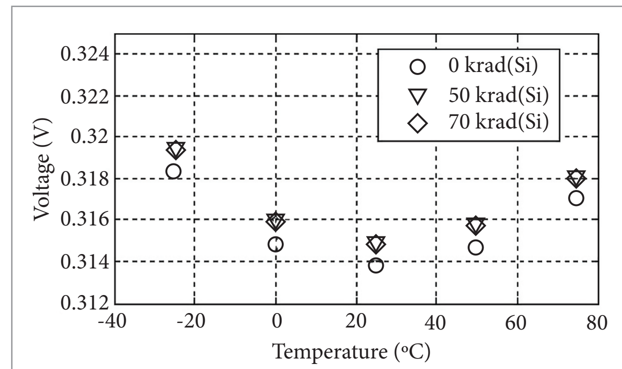

Figure 7. Output voltage for reference 1.

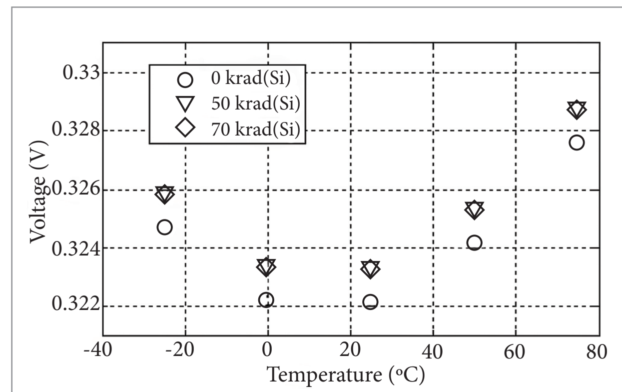

Figure 8. Output voltage for reference 2.

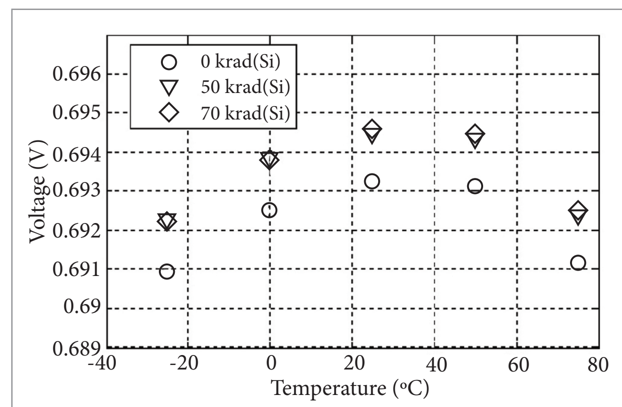

Figure 9. Output voltage for reference 3.

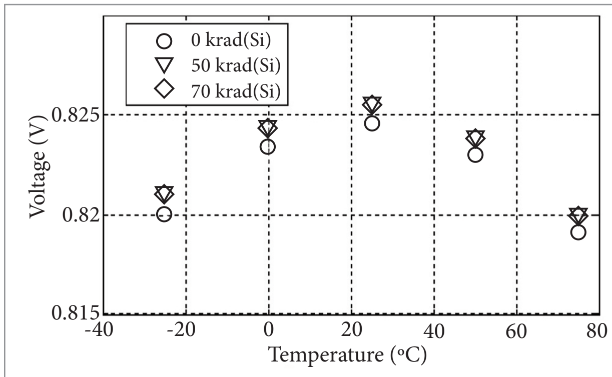

Figure 10. Output voltage for reference 4.

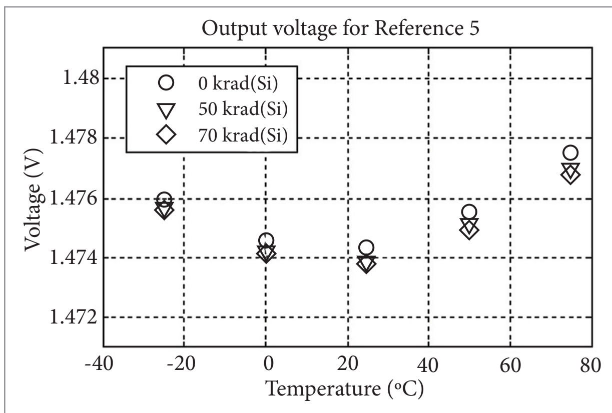

Figure 11. Output voltage for reference 5.

The simulation results indicate that for the 0.13 µm technology voltage references, total ionizing dose is not a major concern. Compared with pre-irradiation simulations, both 50 and 70 krad simulations for the five voltage references showed shifts of a few millivolts in the average output voltage. The standard deviation compared with the pre-irradiation, which considers only process variability, increased by a few millivolts under total ionizing dose for voltage references 1, 2, 3 and 5. On the other hand, voltage reference 4 experienced a decrease of the standard deviation under TID. This reduction was also observed when threshold voltage shifts due to total ionizing dose were applied only to the NMOS transistor M_{R1}, as shown in Fig. 5. The mechanism responsible for this reduction of the standard deviation, however, was not identified.

The observed overall reduction in the standard deviation between 50 krad and 70 krad was expected due to the fact that the standard deviation of the threshold voltage shift data from Haugerud *et al.*, (2005) is reduced between 50 krad and 70 krad, regardless of the fact that the average shift increases.

Table 1. Standard deviation of the output voltage for 0 krad (Si).

Voltage references	Temperature			
	-25°C	0°C	25°C	50°C
1 (mV)	14.7	14.9	15.2	15.4
2 (mV)	14.6	14.9	15.2	15.6
3 (mV)	27.8	28.2	28.8	29.2
4 (mV)	32.0	32.3	32.7	33.1
5 (mV)	23.8	25.5	27.2	29.2

Table 2. Standard deviation of the output voltage for 50 krad (Si).

Voltage references	Temperature			
	-25°C	0°C	25°C	50°C
1 (mV)	18.0	18.2	18.5	18.8
2 (mV)	16.2	16.5	16.9	16.9
3 (mV)	28.1	28.6	29.1	29.6
4 (mV)	27.9	28.2	28.6	29.1
5 (mV)	25.5	21.2	29.0	31.0

Table 3. Standard deviation of the output voltage for 70 krad (Si).

Voltage references	Temperature			
	-25°C	0°C	25°C	50°C
1 (mV)	16.6	16.7	17.0	17.2
2 (mV)	15.6	15.9	16.2	16.5
3 (mV)	28.0	28.5	29.0	29.5
4 (mV)	27.8	28.1	28.5	28.9
5 (mV)	24.7	26.3	28.1	30.0

The average output voltage for all voltage references also presented a small variation between 50 and 70 krad compared with the variation observed between 0 rad and 50 krad. This is expected due to similar threshold voltage shifts for such doses.

The results obtained in this work indicate that these voltage references are functional for doses of approximately 70 krad (Si), and are hence suitable for most space applications. The standard deviation increase of the output voltage due to TID effects, however, should also be considered in order to guarantee proper circuit operation. It is necessary to observe, however, that the data regarding

threshold voltage shifts due to TID, employed in simulation, were not obtained for the 0.13 μm IBM technology. Further irradiation tests are necessary to confirm the simulation results.

In addition, the simulations performed in this work did not take circuit layout into consideration. This is an important issue considering that circuit layout techniques, such as the layout of an enclosed gate for NMOS transistors to reduce leakage current beneath the bird's beak region (Mavis and Alexander, 1997), affect radiation tolerance.

CONCLUSIONS

The five voltage references simulated in this work presented tolerance to total ionizing dose effects for doses of approximately 70 krad (Si). For the simulated 0.13 μm technology, parametric shifts due to TID effects resulted in shifts of a few millivolts in the output voltage of voltage references, and in the standard deviation of the output voltage. Despite the positive results in simulations, irradiations tests are required, as circuit layout, for instance, was not accounted for during simulation.

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