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Novel Design of a Hybrid Superconducting Fault Current Limiter with Controlled Solid-State Device

Henrique K. Miyamoto, André T. Queiroz, Daniel H. N. Dias, Bruno W. França, Felipe Sass, Guilherme G. Sotelo
Universidade Federal Fluminense, NITEE- Núcleo de Inovação Tecnológica em Engenharia Elétrica, Passo da Pátria St. 156, E-347, Niterói-RJ, Brazil
hkmiyamoto@id.uff.br, andretqueiroz@gmail.com, dhndias@id.uff.br, bwfranca@id.uff.br, felipesass@id.uff.br, gsotelo@id.uff.br

***Abstract*— Fault current limiters are essential devices used to protect the power system and its equipment against high levels of fault current, which are growing up due to the increase of new power sources. This paper proposes a novel design of a Hybrid Superconducting Fault Current Limiter (Hybrid SFCL), which is composed basically by thyristors in series with a superconducting element. This branch is connected in parallel to an air-core reactor, which improves limitation and ensures the safe operation of the superconductor element. Another advantage of this topology is the use of the voltage drop in the superconductor as an input parameter to the controller. This voltage is used to detect the fault, which avoids the need for a current sensor and, consequently, reduces the manufacturing costs. In this work, the PSCAD/EMTDC software was employed to modeling the Hybrid SFCL and the 2G superconducting tape, which was modeled considering the thermal-electrical analysis. The results show that the fault current is efficiently limited, and the developed controller strategy has shown a relatively good performance. Furthermore, the proposed system guarantees a fast recovery time, in the order of 500 ms, which is a good advantage when compared to the conventional resistive SFCL.**

***Index Terms*—**Fault current limiter; Power system protection; Substation protection; Superconducting materials.

I. INTRODUCTION

With the integration of new power generation systems, including renewable energy sources in the distribution system, the short-circuit level has increased. Furthermore, the power generation is not growing proportionally to the demand, which leads the system to operate close to its capacity limits [1]–[4]. These conditions may result in fault situations that exceed the scaled levels for equipment that compose the electrical power system. One way to solve this problem is to scale up all the distribution substations, by replacing the main equipment, such as power transformers, protection systems, and automatic recloser. However, this solution can be too expensive and, in most cases, is not applicable. A more efficient and interesting solution is to use a Fault Current Limiter (FCL) [5]–[8], which reduces the fault current levels to a suitable value, thus avoiding the need to scale up the substation [9]–[11]. The FCL is capable of operating with negligible impedance during normal system

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conditions, and during a fault event, it changes to a high resistive value in normal state, limiting the current to a reduced value.

The ideal characteristics of an FCL are: fast acting current limiting device, reduced recovery time, operating reliability, lower installation and maintenance costs, low loss and negligible impedance in normal operation, and a reduced volume and weight [12].

Among the technologies found in the literature [12], the Solid-State Fault Current Limiter (SSFCL) [13], [14] is presented as a promising solution for the application in power distribution systems. The SSFCL can be classified into three main groups [14]: series type [15], bridge type [7], [16], and resonant type [4].

Another solution that has been recently studied and experimentally applied is the Superconducting Fault Current Limiter (SFCL) [17]–[19]. Based on second generation (2G) of superconducting tapes [17], the resistive SFCL has the simplest and most compact structure, among other topologies [20]–[22]. The main disadvantage of resistive SFCL is that the superconducting material takes a few seconds to recover its initial state after the fault extinction due to its thermal characteristics. Because of this fact, many works have been proposed trying to reduce the recovery time in resistive SFCL [23], [24].

To combine the advantages of the two topologies mentioned above, a Hybrid SFCL has been proposed and studied by different works [25]–[27]. The Hybrid SFCL topologies described by the references above are designed using superconducting elements and fast switches. The fast conventional switches are specially developed to act in the first cycle or half-cycle of the fault current [26]. However, these switches have complex construction and a negative impact for reliability of this equipment [28]. The topology proposed in this paper replaces the conventional fast switches by semiconductor ones, and the developed control algorithm uses the voltage drop that appears in the superconductor material during its thermal transition [29]. Moreover, the use of voltage sensing aims to reduce the cost in the final price of the equipment, since the superconducting element transition indicates the occurrence of a fault event.

For this study, the Hybrid SFCL was simulated in PSCAD/EMTDC software. The 2G tape was modeled using a thermal-electrical approach, and it was validated comparing to the results with the experimental results found in previous work [30].

This article is organized into five sections. After the introduction presented here, Section II presents the proposed Hybrid SFCL topology and its modeling. Section III and IV show the simulated cases and results, respectively. Finally, in Section V, the conclusion is presented.

II. HYBRID SFCL TOPOLOGY

Hybrid SFCLs are normally composed of a superconducting material, a switching component (it may be a fast switch or a solid-state device), and a shunt component to limit the fault current and dissipate the power. The combination of the superconducting material and the solid-state switch

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device (thyristors, in the case of this work) in the same equipment can keep the advantages of each technology and avoid the problems encountered in both.

The proposed Hybrid SFCL, shown in Fig. 1, is composed of antiparallel thyristors in series with a 2G tape (variable resistance - R_{tape}). This branch is connected in parallel to an air-core reactor (L), which improves limitation and ensures the safe operation of the superconductor element.

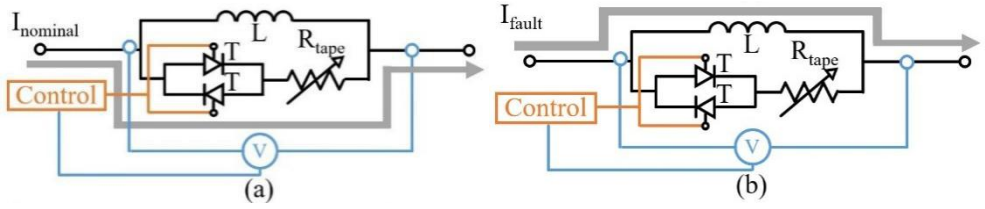

Fig. 1. Simplified hybrid SFCL circuit in (a) the normal operation and (b) during fault conditions.

The operation of the proposed Hybrid SFCL is given, according to Fig. 1, as follows. In steady-state, the system current flows through the thyristors and the superconducting element (R_{tape}), as shown in Fig. 1(a). When the fault occurs, the current increases, and it starts the superconducting transition. During this process, a voltage drop appears in the superconductor material as fast as the current increases due to the intrinsic characteristics of these materials. The voltage drop is used as a control parameter for the thyristors, and they are commanded to open. Thereafter, the current derives to the shunt reactor, which limits the fault current, as showed in Fig. 1(b). The voltage measurement is performed in the Hybrid SFCL terminals and its value compared to the limit values. When the threshold is exceeded, the thyristors receive the open command signal. However, due to the characteristics of this switch, it will open only when the current crosses the zero value. During this time, the fault current will circulate entirely through the superconducting element, which will be responsible for the limitation itself. Note that without the superconducting element, the fault current will not be limited during the first half-cycle, and the system may have some electromechanical stress problem.

In a previous work of the authors, the superconducting element used in the proposed Hybrid SFCL topology was studied [31], and it was simulated using the thermal-electrical analogy that can be found in references [19], [30], [32]. As shown in [33], the superconducting element was built using a 2G tape manufactured by Super Power Inc., 12 mm width, a critical current of 275 A at 77 K and a critical temperature of 92 K [33]. The 2G tape is composed of four layers with different sizes and materials. The superconducting layer is composed by Yttrium Barium Copper Oxide (YBCO), which corresponds only to 10% of the total 2G tape (0.1 mm thickness). Two silver layers (just for covering and protecting the superconducting material) and a Hastelloy layer, which gives a mechanical stabilization to the final tape, compose the majority part of the tape.

For this work, the PSCAD/EMTDC software was chosen to simulate the Hybrid SFCL applied in a simplified system. For the 2G tape model, the thermal-electrical analogy is implemented using the FORTRAN programming language. Therefore, this model reproduces the thermal and electrical

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behavior of the superconductor element. Moreover, this software allows evaluating the limiter operation in an electrical network represented by its Thévenin equivalent.

A. Electrical Model

To determine the 2G tape electrical behavior, firstly, four variable resistors in parallel are considered, which represents each layer individually. All the resistances and other parameters like current, resistivity, and temperature, for example, have the subscript corresponding to the layer (n), as represented in Fig. 2.

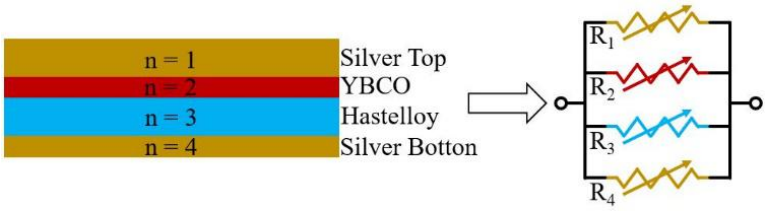

Fig. 2. Cross-section of the tape 2G YBCO and its electrical representation [19], [30], [32].

The electrical resistivity of the materials has a linear behavior concerning the temperature, except for the YBCO when it is below its critical temperature ($T_c = 92$ K) since it shows a non-linear relation [34]. The electrical resistivity functions in (Ω.m), of the silver and Hastelloy material, are described in equations (1) and (2) respectively, where $T_{1,4}$ and T_3 are the temperatures, in Kelvin, of each silver layer (layers 1 and 4) and the Hastelloy layer (layer 3).

$$\rho_{1,4} = (-2{,}082 \cdot 10^{-7}) + (6{,}17 \cdot 10^{-9} \cdot T_{1,4}) \quad (1)$$

$$\rho_3 = (-1{,}103 \cdot 10^{-7}) + (8{,}958 \cdot 10^{-9} \cdot T_3) \quad (2)$$

The behavior of the YBCO electrical resistivity is different when the temperature is above or below T_c. At temperatures below T_c ($T_2 \leq T_c$), the resistivity is a function of the electric field (E) and the current density (J), through a relation known as the *E-J* curve [32] and mathematically expressed in (3). At temperatures higher than T_c ($T_2 > T_c$), the YBCO electrical resistivity is a linear function of temperature, as expressed in (4).

$$\rho_2 = E/J\,,\ (T_2 \leq T_c) \quad (3)$$

$$\rho_2 = -0{,}1 + (10^{-2} \cdot T_2),\ (T_2 > T_c) \quad (4)$$

The electrical resistance of each layer is described in equation (5), where d_n, l_n, and e_n are the length, width, and thickness of the n-layer, respectively. The calculation of the equivalent resistance R_{tape} is expressed in equation (6).

$$R_n = \rho_n \cdot [d_n/(l_n \cdot e_n)] \quad (5)$$

$$\frac{1}{R_{tape}} = \left(\frac{1}{R_1}\right) + \left(\frac{1}{R_2}\right) + \left(\frac{1}{R_3}\right) + \left(\frac{1}{R_4}\right) \quad (6)$$

The expression for the current of each layer (i_n) is given by equation (7), which can be obtained through a simple current divider, and i_{tape} is the total current flowing through the 2G tape.

$$i_n = (R_{tape}/R_n) \cdot i_{tape} \quad (7)$$

For the current calculation, the use of an iterative method is necessary, due to the non-linearity of the superconductor (*E-J* relation) during its phase transition. Fig. 3 shows a flowchart summarizing

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the iterative process for calculating the electrical resistivity and the current in the superconducting element.

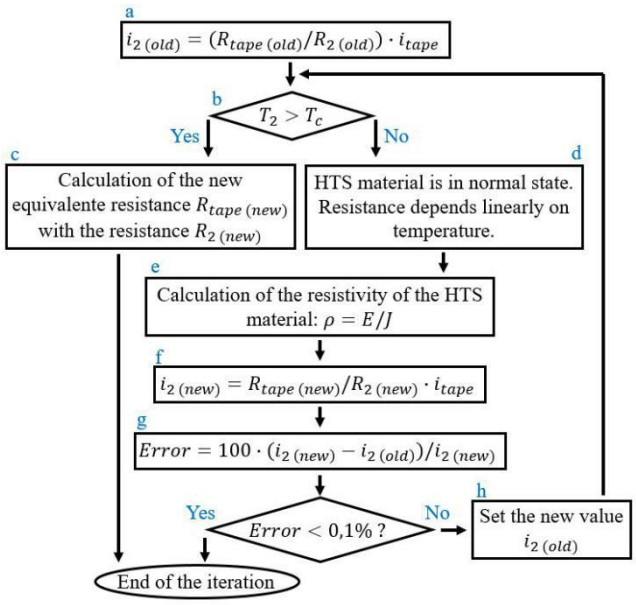

Fig. 3. Flowchart of the iterative process of resistivity and electric current in the superconductor. Adapted from [30], [32].

For a current $i_{2(old)}$ (step "a") flowing through the superconductor, the YBCO temperature value T_2 is compared with T_c (step "b"). If T_2 is greater than T_c, then the material is in the normal state, wherein the resistivity of the YBCO layer is calculated using (4). The other resistivities are calculated using equations (1) and (2), and the resistances through equations (5) and (6), and the iterative process is finished (step "c"). Otherwise, if T_2 is smaller than T_c, the YBCO resistivity is given by equation (3) (step "d"), and the resistors R_2 and R_{tape} are updated by equations (5) and (6), respectively (step "e"). The new value for the current flowing through the superconducting $i_{2(new)}$ is calculated (step "f"), and the error between $i_{2(old)}$ and $i_{2(new)}$ is determined (step "g"); if the *Error* is less than the tolerance of 0.1%, it is considered stable, and the process ends. If it is higher than the tolerance, the $i_{2(old)}$ value is incremented by a variable adjustment factor, which considers the *Error* behavior during the whole processes [32], and the iterative process will repeat until the *Error* is less than 0.1%.

B. Thermal Model

As mentioned before, to obtain the temperature of each layer at each step during the fault transient, a thermal-electrical analogy is proposed [30], [32]. The fundamental purpose of this approach is to determine the variable electrical resistivity associated with the material temperature. Another advantage of this analogy comparing to the classical thermal equation is the simplicity to implement in PSCAD software, which improves the transient electrical calculation.

For this approach, it was considered that the temperature (T_n) varies only in one direction (1D) along with the thickness (e_n) of each layer of the 2G tape, as shown in Fig. 4, wherein the T_5 is the liquid nitrogen temperature (77 K). The temperature can be defined by the analogy between the 1D transient heat conduction equation, as shown in (8) (thermal variables), and the discrete RC circuit

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equivalent to the transmission line equation, in (9), with the equivalent electrical variables. The thermal-electrical circuit can be seen in Fig. 5, wherein the source of DC voltage (77 V) represents the environment temperature, where the 2G tape is cooled by liquid nitrogen at 77 K (V_5).

$$\frac{\partial T}{\partial t} = \frac{\lambda}{\gamma c} \cdot \frac{\partial^2 T}{\partial z^2} + \frac{g}{\gamma c} \tag{8}$$

$$\frac{\partial v}{\partial t} = \frac{1}{R \bullet C} \cdot \frac{\partial^2 v}{\partial z^2} + \frac{P}{R \bullet C} \tag{9}$$

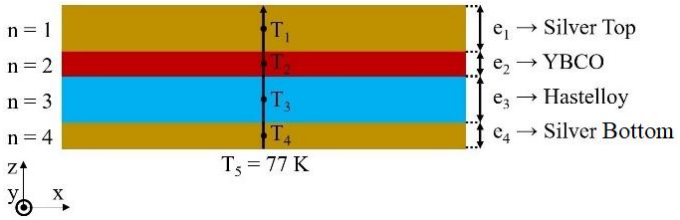

Fig. 4. Temperature variation within a cross-section of the superconducting tape layers. Adapted from [19], [30], [32].

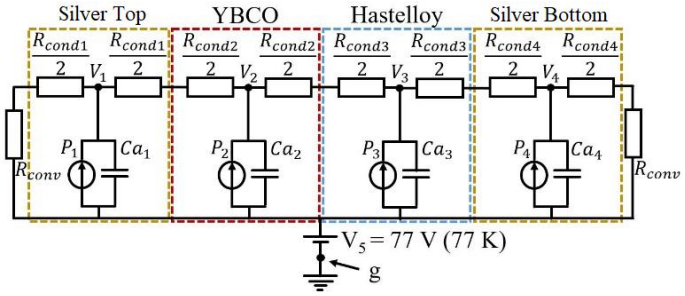

Fig. 5. Thermal-electrical equivalent for the 2G tape. Adapted from [19], [30], [32].

Regarding the equation (8), T is the 2G tape temperature, in Kelvin, t is the transient time (s), λ is the thermal conductivity at this point ($W/K.m$), z is the considered axis (m), γ is the specific mass of the material (kg/m^3), c is the specific heat of the material ($J/(kg.K)$), and g is the rate of internal heat generation into material (W/m^3). Considering equation (9), v is the voltage (V), R is the resistance (Ω), C is the capacitance (F), and P is the power (W) provided by the current source. It is noteworthy that the heats transfer along the x and y-axis were not considered, only the temperature gradient in each layer thickness along the z-axis. The current sources connected in parallel to the capacitor denotes the internal heat generation in each layer, highlighted in [32].

The following analogies for the electrical and thermal parameters, as shown in equations (10) to (13), were considered. The electrical parameters such as the voltage (V_n), the conduction and convection resistance ($R_{cond\ n}$ and R_{conv}), and the capacitance (Ca_n) represents, respectively, the following thermal parameters: temperature (T_n), the inverse thermal conductance, the convective transfer and the thermal capacity. Moreover, the current source value is given by the internal heat generation, which is expressed in terms of the electrical resistance (R_n), as written in equation (14).

$$V_n = T_n \tag{10}$$

$$R_{cond\ n} = l_n/(\lambda_n \bullet d_n \bullet l_n) \tag{11}$$

$$R_{conv} = 1/(h_n \bullet d_n \bullet l_n) \tag{12}$$

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$$Ca_n = \gamma_n \bullet c_n \bullet d_n \bullet l_n \bullet e_n \tag{13}$$

$$P_n = R_n \bullet i_n^2 \tag{14}$$

Applying Kirchhoff's law to the central nodes shown in Fig. 5, it can be obtained the voltages values V_1, V_2, V_3, and V_4 and, consequently, the temperature values T_1, T_2, T_3, and T_4.

C. Solid-State Device Modeling

Solid-state switches have some disadvantages compared to electromechanical ones, such as the need for an electronic control circuit and a power drive, and the losses presented in conducting state. However, their usage is justified by their superior performance and reduction of implementation and maintenance costs that give a better cost/benefit ratio. Regarding the proposed Hybrid SFCL simulation, the chosen solid-state switch (thyristor) is already modeled in PSCAD/EMTDC software.

III. SIMULATION

In this section, the superconducting element model is employed to validate the proposed Hybrid SFCL topology and its controller. This model was developed in PSCAD/EMTDC software as described in the previous section. Fig. 6 shows the circuit simulation with the components of Hybrid SFCL, which is composed in two main branches. The first one, called the superconducting element branch, is composed of the antiparallel thyristors in series with the 2G tape. The second one is the branch with the air-core reactor used to limit the fault-current (shunt element). This air-core reactor is modeled with a resistor and an inductor in series. To employ the Hybrid SFCL model in an electrical system, it was considered an equivalent 13.8 kV feeder based on a real distribution system, which has a load impedance and a fault impedance described in Table I. This scenario is the maximum fault current case, which has a first asymmetric peak current (I_p) around to 6.0 kA_{peak} and a symmetric current (I_s) around to 2.5 kA_{rms}. The air-core reactor was specified to reduce the prospective fault current in 60%, and the values in Table I were calculated as indicated in [35].

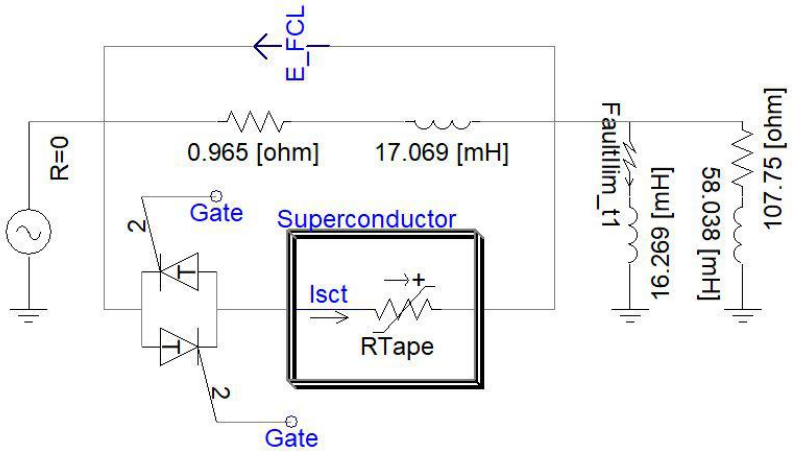

Fig. 6. Proposed Hybrid SFCL simulation in PSCAD/EMTDC software.

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TABLE I. SIMULATION PARAMETERS.

Parameters	Values	
Voltage	13.8	kV_{rms}
Frequency	60	Hz
Load Impedance	107.75	Ω
	58.038	mH
Fault Impedance	0.579	Ω
	16.269	mH
Air Coil Impedance	0.965	Ω
	17.069	mH
Duration of run	1.0	s
Solution Time Step	10.0	µs
Channel Plot Step	10.0	µs

A. Superconducting Tape

Based on the statements presented in Section II.A., it is possible to model the thermal and electrical characteristics of the 2G tape. This model reproduces the tape behavior in both transient and steady-state conditions, which are necessary to study the Hybrid SFCL when submitted to a fault current. For the modeling, a new component was created in PSCAD/EMTDC (Fig. 7 (a)) with its behavior is described by a FORTRAN code. This component has two input parameters, V_{base} and I_{critic}, which are the grid voltage base and the critical current of the 2G tape, respectively. The V_{base} is used to define the length of the tape. In this work, the line-to-line voltage base (V_{base}) is 13.8 kV, and the maximum electric field allowable for the 2G tape is 0.5 V/cm, as indicated in [33]. As a result, approximately 160 m of superconducting tape is needed for the limiter. The critical current of selected 2G tape is 275 A.

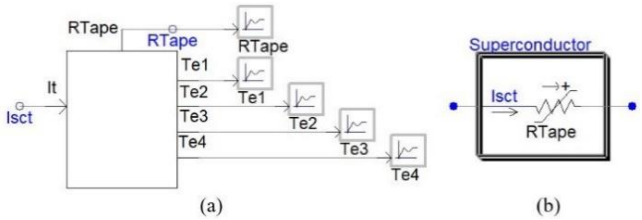

Fig. 7. (a) Component created in PSCAD/EMPTDC to calculate the resistance of the superconducting tape and (b) variable resistance.

The FORTRAN code is processed at each time step with the following steps:

- Read the tape current $I_{sct} = I_{tape}$ (code input);
- Calculate the resistivity and electrical resistance of each layer, $\rho_{1,3,4}$ and $R_{1,3,4}$, according to (1), (2), and (5), except for the YBCO layer;
- The iterative process to calculate the resistivity of the superconductor material, its resistance, and current, ρ_2, R_2, and i_2, according to the flowchart of Fig. 3;
- Calculate R_{tape}, according to (6);
- Calculate the thermal parameters of each layer based on the previous temperature, $R_{cond\ n}$, R_{conv}, ca_n and p_n, according to (11) until (14);
- Calculate the current passing through the other layers, I_n, according to (7);

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- Calculate the temperature in each layer, T_n, based on the thermal-electrical analogy (10), were V_n is obtained through a matrix solution of the equivalent circuit shown in Fig. 5.

The temperature T_n is calculated by applying the nodal analysis method in the circuit of Fig. 5, and then determined a system of partial time differential equations. Since it is a system of coupled equations with more than one independent variable (temperature), as a function of the same independent variable (time), the Euler's method is applied for solving ordinary differential equations, as demonstrated in [32]. Furthermore, the implicit method is adopted with not minimal step-time (*dt*) to achieve numerical stability.

The output of the code is the value of the variable resistor (R_{tape}), depending on the current flowing through it (I_{sct}), both depicted in the equivalent circuit of Fig. 7 (b). It is important to highlight that the temperatures of the layers need an initial condition to be defined by the user. In this work, they are set at 77 K for all layers. Therefore, the variables used for calculation in each step are based on the previously calculated values in the current step or the values defined in the previous step.

For validation purposes, the results of the superconducting tape model obtained in this study were compared to the results in [30], [32], which were validated based on experimental tests of the tape. The simulation results of the tape converge to the same values, and then this is enough to validate the model developed in PSCAD/EMTDC. In this way, subsequent simulations of the Hybrid SFCL can be carried out assuming suitable behavior of the tape in both transient and steady-state conditions. These validation results are not presented here because they are not the main aim of the study.

B. Hybrid SFCL Control

Fig. 8 shows the triggering circuit for firing the thyristors used in the proposed Hybrid SFCL topology. The control works as follows: the voltage between the limiter terminals (*E_FCL*) is compared to a predetermined threshold in block "A". If *E_FCL* cross the threshold value, the limiting mode is activated, and the gate signal is set to low-state to order switching off. To restore the normal operation, besides the condition of E_FCL lower than the threshold value, a time delay is imposed to ensure that the superconducting material returns to 77 K. A logical operator (AND) and a time delay block (block "B") are used to provide such functionality, as shown in Fig. 8.

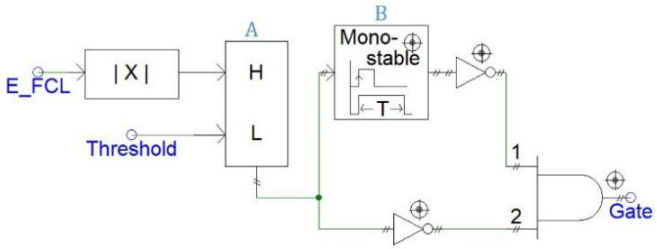

Fig. 8. Switching control.

The threshold is defined according to the peak-voltage of the limiter operating in the limiting mode, within the minimum value obtained in the presence of a fault and the maximum value obtained after the fault is cleared. This range avoids the improper operation due to overvoltage and ensures the

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transition to the normal mode when the fault is cleared. The aforementioned values are obtained through simulations considering the possible variation of the system parameters. In this work, the minimum peak-voltage of the limiter operating in the limiting mode and in the presence of a fault is 10.0 kV. The maximum peak-voltage of the limiter operating in the limiting mode and after the fault is cleared is 1.2 kV. The threshold value is set as 2.0 kV.

IV. RESULTS

A. Currents in Hybrid SFCL

Fig. 9 shows the simulation results for a fault at 0.1 s. In this figure, the green curve is the prospective curve (fault current without the limiter); the blue curve is the limited curve; the red curve is the current through the thyristor and 2G tape branch, and; the pink curve indicates the gate triggering, i.e., control order to the limiter. The red curve shows the main advantage of the proposed topology. As the superconducting element transits in a fault condition, the fault current is already limited before passing through the air-core reactor branch (less than a quarter of half-cycle). Hence, the thyristor can switch off before the end of first half-cycle of limited current (blue curve). Therefore, the first peak of the limited current is 2.89 kA_{peak}, which represents a 51.56% reduction from the 5.61 kA_{peak} prospective curve. The steady-state current shows 1.58 kA_{peak} for the limited current, which represents a 47.13% reduction from the 3.35 kA_{peak} prospective curve.

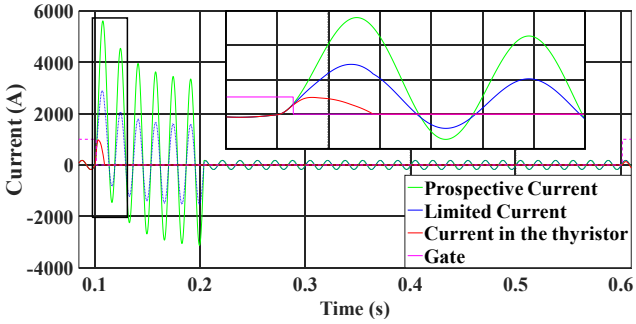

Fig. 9. Currents in hybrid SFCL.

The association of the instantaneous current limitation provided by the superconducting element with the faster switching off provided by the thyristors, the proposed topology enhances the FCL performance when compared with both conventional SFCL and SSFCL. The superconducting element transition enables a current limitation in the first half-cycle, overcoming the limitation of the solid-state FCL topology due to the thyristor switching characteristic. The thyristors' operation after the end of fault current half-cycle protects the 2G tape, in the superconducting element branch, to be exposed at long time high-level currents and then ensuring increased durability and faster recovery time.

It is important to note that the proposed controller ensure that the fault current is clear, and the 2G tape lies in the superconducting state before switching on the thyristors to operate the limiter in the normal mode again. This is the reason for the control signal was applied only at 0.61 s.

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B. Control Analysis

In Fig. 10, the relationship between fault current and the voltage used for controlling the switches is presented. In this study, the voltage threshold is set at 2 kV. When this threshold is reached, the instantaneous current flowing through the limiter is approximately 672 A. This current is higher to the nominal current of 13.8 kV feeder (125 A_{rms}) being considered as a fault-current level. At 0.2 s the fault is extinguished, and the voltage level is again below the threshold. However, the superconducting element has to recover from the transition. In this way, a 500 ms delay is imposed to ensure the recovering process.

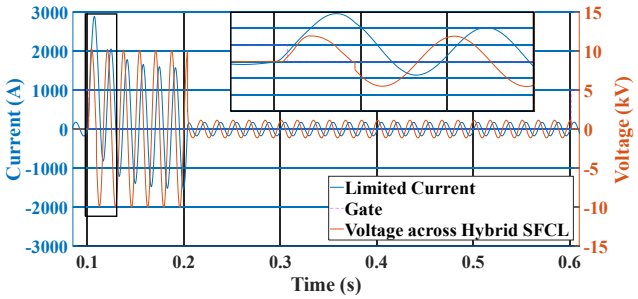

Fig. 10. The controlling relationship between current and voltage.

In the graph, the orange curve is the voltage at the limiter that switches from 10.1 kV to 1.2 kV, considering the parameters mentioned in this work and the driver acting range explained in Section III.B.

C. The Temperature of the Superconducting Element

Since the superconducting element has been modeled concerning the electrical and thermal characteristics, it is possible to obtain the temperature rise of each layer by simulation, as showed in Fig. 11. It was observed that the temperature reaches 95.86 K and as soon as the fault was cleared, a fast temperature reduction occurs due to the opening of the superconducting element branch. Hence, the superconducting element takes about 500 ms to return to the steady-state (77 K). This is the time delay necessary to ensure the material return to the superconducting state, applied in the control to restore the normal operation even if the fault is already cleared.

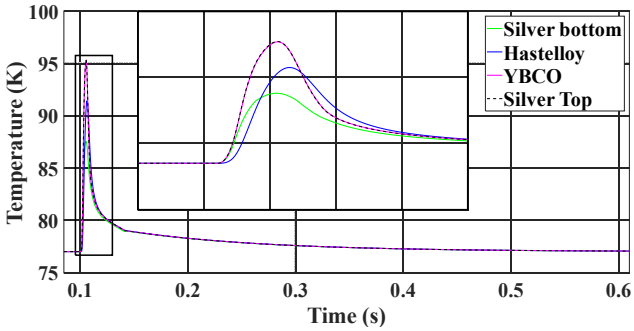

Fig. 11. Temperature rise of each of the superconducting layer - using thyristors.

D. Comparison Between the Proposed Hybrid SFCL and Conventional SFCL

To evaluate the benefits of the proposed topology comparing to the conventional SFCL, the thyristors were replaced by an ideal circuit breaker with an open time delay. This delay was used to

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emulate the time of mechanical circuit breakers, set at 50 ms [36]. For the control system, the same logical proposed in this paper was used. In Fig. 12, the first peak remains to the same behavior as observed in Fig. 11 since the superconducting element transits to the normal state. The difference is evident after the first peak. Because the time delay to clear the fault current at the superconducting element branch, the superconductor temperature lies above the critical temperature (92 K). This high temperature may require a higher length of 2G tape and reduces its lifetime when compared to the proposed topology.

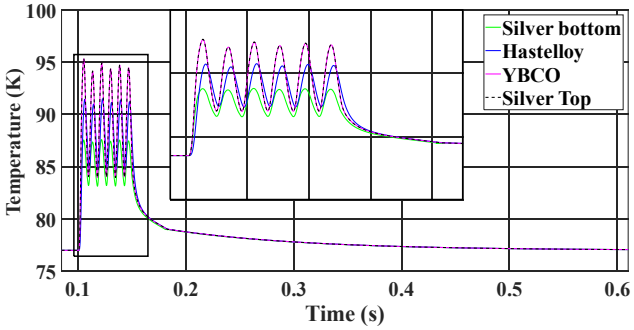

Fig. 12. Temperatures of the superconducting layers - Limiter with emulated mechanical switch.

In Fig. 13, the limited curves are compared. Until the thyristor switches off, both limited curves have the same behavior since the current is through in the superconducting element and the air-core reactor. After the thyristors open, only the air-core reactor is limiting the current in the proposed Hybrid SFCL, whereas the conventional SFCL takes about 50 ms to open. Thereafter, they return to exhibit the same limited current behavior. It noted that the high superconducting resistance in the normal state make the difference between these two topologies not huge. Nevertheless, other effects like electrical arcing by opening a conventional circuit breaker, mechanical stress and the power dissipation in the 2G tape must be considered.

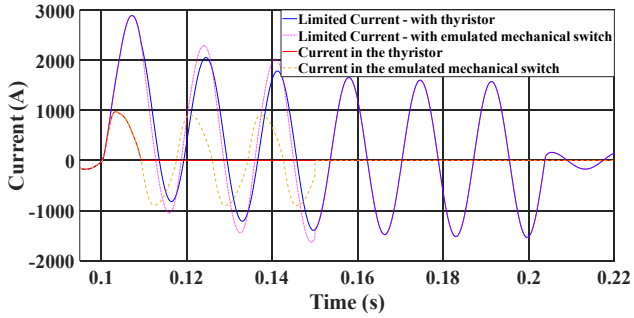

Fig. 13. Limited current using thyristors and emulated mechanic switch.

V. CONCLUSION

This paper proposed a Hybrid SFCL topology to enhance the limiting performance and to combine the benefits of the SFCL and the SSFCL. The control is based on the measured voltage at the terminals of the limiter, so a voltage sensor is possible to applied due to the transition of states of the superconducting element. The voltage drop along the 2G tape occurs when the current is above its critical value (e.g., a fault condition). This transition results in an increased voltage at the limiter

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terminals. Hence, it avoids the need for a current sensor that could be more expensive than the proposed sensor. The hybrid topology provides a faster opening of the superconducting element branch, which reduces its recovery time, avoids the need for a huge 2G tape length, and improves its lifetime.

The superconducting element was modeled in PSCAD/EMTDC software. This model considered the thermal-electrical characteristic of the 2G tape. The simulation results with the proposed Hybrid FCL showed that the fault current is limited less than a quarter of half-cycle, even using the thyristors. This is possible because the current in the superconducting element branch is already limited before flowing through in the air-core reactor branch, which represents the majority of the limited current. The proposed limiter was compared with a conventional SFCL using an emulated electromechanical circuit breaker. Simulation results showed that the proposed Hybrid FCL has a better performance in the transient condition of the fault.

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