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High Efficiency Continuous Inverse Class-F Power Amplifier with Modified Current Waveform

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***Abstract*— Continuous inverse class-F (CICF) is a recent mode of harmonically-tuned RF power amplifiers used to extend the operating bandwidth of the conventional narrowband class-F^{-1} power amplifier by producing variable set of drain current waveforms and load admittances that give the same operating efficiency. In this work, a new approach of analysis is developed by suggesting some modified drain current waveforms and comparing the resulting theoretical performance characteristics such as drain efficiency and output RF power with the conventional type. It has been shown that the drain current with a truncated square wave shape can better model the actual behavior of the power amplifier, delivering a theoretical efficiency higher by about 8% than the conventional shape. Besides, a simple analytic technique for extracting the device harmonic load impedances for the desired band is also presented. Based on the theoretical analysis, a 6 W power amplifier circuit was designed and simulated to operate within the frequency band 800 – 1000 MHz. Simulation results indicated that a drain efficiency of values between 82% and 86% was obtained across the specified band.**

***Index Terms*—** Continuous Inverse Class F, GaN HEMT, High Efficiency PA, Harmonic Load Network.

I. INTRODUCTION

RF power amplifiers are key elements in modern mobile radio systems. Their most significant design characteristics are DC-to-RF efficiency, output RF power, linearity, and operating bandwidth. However, achieving all these desired requirements is usually difficult and therefore compromise is carried out depending on the specific application. Harmonically-tuned power amplifiers such as class-F [1] and class-F^{-1} [2] are well-known high efficiency amplification techniques used extensively to amplify signals with achievable efficiencies of greater than 80%, thereby reducing heat sink size and increasing battery life in mobile transmitters. The design philosophy of these amplifiers is based on reshaping the active device's output voltage and current waveforms for minimum overlapping by controlling some finite number of harmonics through presenting short or open circuit terminations at these harmonics [3]. However, the stringent singular-point impedances are difficult to achieve over a wide range of frequencies and therefore these types of power amplifiers cannot satisfy the bandwidth requirements for modern high data rate schemes used in LTE and 5G wireless systems.

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Over the past two decades, continuous mode harmonically-tuned power amplifiers such as class-J [4], continuous class-F (CCF) [5], and continuous inverse class-F (CICF) [6] have been developed to provide both broadband and efficient operation. In the continuous inverse class-F mode, the fundamental and second harmonic load admittances are allowed to vary over a specified range of values while keeping the same RF performance. This technique introduces a flexible design space instead of presenting open or short-circuit impedances, thereby permitting wider bandwidth. An extended mode for the continuous inverse class-F power amplifier was proposed by introducing a new flexible design space through varying the resistive part of the second harmonic impedance [7]. Successful realizations of broadband continuous class-F^{-1} power amplifier circuits were carried out using harmonic load networks with Chebyshev [8] and elliptic [9] low pass structures. A modified continuous class-F^{-1} power amplifier with variable third harmonic load impedance was also suggested to extend the design space and make the implementation of the load network more realistic [10]. The effect of the current conduction angle on the RF performance parameters of the continuous class-F^{-1} power amplifier was also studied [11].

In this paper, new alternative ways to model the drain current waveforms are presented. The resulting performance parameters are evaluated and compared with the conventional mode of the continuous inverse class-F power amplifier. An analytic approach for estimating the optimum load impedances in terms of the active device's parasitic elements is also developed. The proposed analytic approach provides better estimation for the required fundamental and harmonic load impedances and thereby introduces closer theoretical prediction for efficiency and RF performance when compared with the conventional CICF power amplifier analysis developed originally by Carrubba *et al.* [6].

II. Theory of the Continuous Inverse Class-F Mode

A typical simplified equivalent output circuit for the GaN HEMT is shown in Fig. 1, where both the most effective intrinsic and packaged elements are presented. The output nonlinear capacitance C_{ds} is a voltage dependent element and is a part of the intrinsic bare-chip device model. On the other hand, the parasitic package elements are represented by two LC sections.

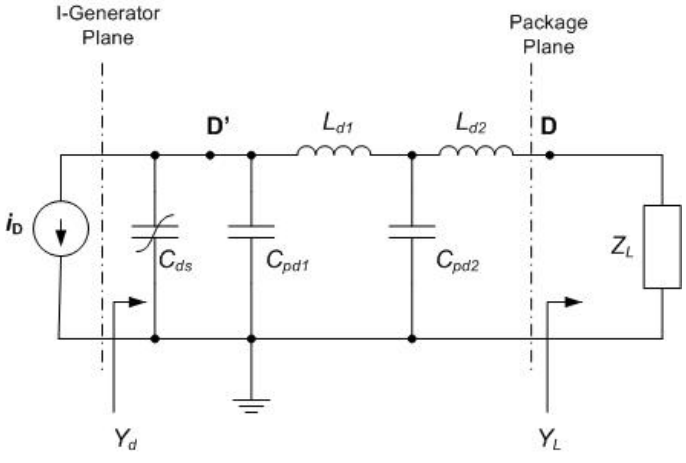

Fig. 1. Simplified Output Circuit for the GaN HEMT Power Transistor.

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In inverse class-F power amplifier with a finite number of three harmonics, the drain voltage waveform at the current generator reference plane is assumed to be half-sinusoidal [12]:

$$v_D(\theta) = V_{DD}(1 + \sqrt{2}\cos\theta + 0.5\cos 2\theta) \tag{1}$$

where V_{DD} is the drain bias voltage and $\theta = \omega_0 t$, and ω_0 is the fundamental angular frequency.

On the other hand, the drain current waveform composed of DC, fundamental, and third harmonic components is given by [13]:

$$i_D(\theta) = I_{DC}(1 - \frac{2}{\sqrt{3}}\cos\theta + \frac{1}{3\sqrt{3}}\cos 3\theta) \tag{2}$$

where I_{DC} is the DC component of the drain current, and $i_D(\theta) \geq 0$.

Equation (2) can be re-written in terms of the maximum drain current, I_{max}, in the form:

$$i_D(\theta) = I_{\max}(\frac{1}{2} - \frac{1}{\sqrt{3}}\cos\theta + \frac{1}{6\sqrt{3}}\cos 3\theta) \tag{3}$$

In continuous class-F^{-1}, a pattern of drain current waveforms can be obtained by multiplying (3) by another term such that [6]:

$$i_D(\theta) = I_{\max}(\frac{1}{2} - \frac{1}{\sqrt{3}}\cos\theta + \frac{1}{6\sqrt{3}}\cos 3\theta).(1 - \gamma\sin\theta) \tag{4}$$

where γ is an empirical parameter ranging between -1 and 1.

The drain current waveforms, normalized to I_{max}, are sketched in Fig. 2 for three values of the parameter γ, showing a peak drain current $i_{D(\text{peak})} = 1.68\ I_{max}$.

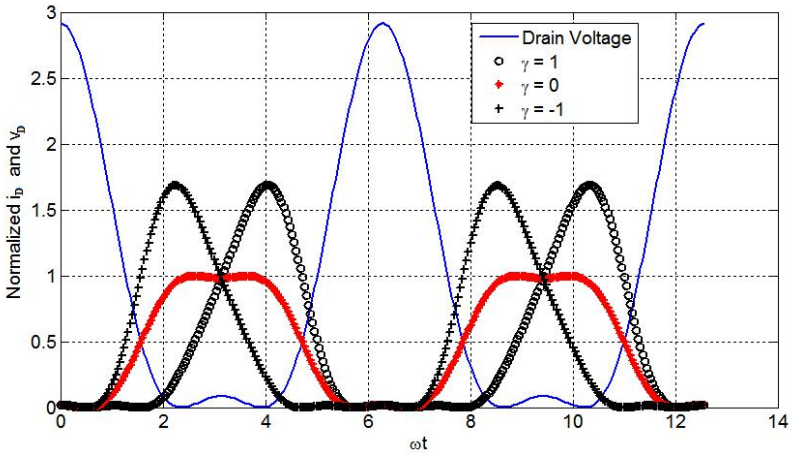

Fig. 2. Drain current waveforms for three values of γ.

Equation (4) can be de-factorized and re-arranged to produce the following first three current harmonic components:

$$I_{d1} = (-\frac{1}{\sqrt{3}} + j\frac{\gamma}{2})I_{\max} \tag{5}$$

$$I_{d2} = -j\frac{7\gamma}{12\sqrt{3}}I_{\max} \tag{6}$$

$$I_{d3} = \frac{1}{6\sqrt{3}}I_{\max} \tag{7}$$

Similarly, the first three drain voltage harmonic components are evaluated from (1):

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$$V_{d1} = \sqrt{2}.V_{DD} \tag{8}$$

$$V_{d2} = \frac{1}{2}V_{DD} \tag{9}$$

$$V_{d3} = 0 \tag{10}$$

The harmonic load admittances at the current generator reference plane of the power FET can be evaluated from:

$$Y_{dn} = -\frac{I_{dn}}{V_{dn}} \tag{11}$$

So, the load admittances are given by:

$$Y_{d1} = (\frac{2}{\sqrt{6}} - j\frac{\gamma}{\sqrt{2}})G_{opt} \tag{12}$$

$$Y_{d2} = j\frac{7\gamma}{3\sqrt{3}}G_{opt} \tag{13}$$

$$Y_{d3} = \infty \tag{14}$$

where $G_{opt} = 1/R_{opt}$, with R_{opt} is the optimum load-line resistance in the class-B mode of operation when all harmonics are assumed to be short-circuited and is equal to $2V_{DD}/I_{max}$.

The DC input power is given by:

$$P_{DC} = \frac{1}{2}V_{DD}I_{\max} \tag{15}$$

The RF output power is evaluated from (5) and (8):

$$P_{out} = \frac{1}{\sqrt{6}}V_{DD}I_{\max} \tag{16}$$

The theoretical drain efficiency can be found from dividing (16) by (15) and is equal to 81.65%. Although this theoretical approach of analysis is clear and simplified but practical realizations of continuous inverse class-F power amplifier circuits achieve drain efficiencies greater than this figure [9,10], revealing the need for a more accurate drain current representation.

III. Modified Drain Current Waveforms

In this section, two new approaches to characterize the drain current waveform in continuous inverse class-F mode are proposed with the derivation of the corresponding load admittances, output RF power and drain efficiency.

A. Drain Current Waveform with 2nd and 3rd Harmonic Tuning

The drain current waveform that is composed of three harmonic components can be expressed in the form:

$$i_D(\theta) = I_{DC}(1 - \zeta_1\cos\theta + \zeta_2\cos 2\theta - \zeta_3\cos 3\theta) \tag{17}$$

where $\zeta_1 = 1.62$, $\zeta_2 = 0.87$, and $\zeta_3 = 0.25$ are the optimum current waveform factors for maximum fundamental current component provided that $i_D(\theta) \geq 0$ [12].

In accordance with (1) and to avoid second harmonic admittance with negative conductance, the above equation can be re-written after contributing an additional phase shift:

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$$i_D(\theta) = I_{DC}(1 - \zeta_1 \cos(\theta - \varphi) + \zeta_2 \cos 2(\theta - \varphi) - \zeta_3 \cos 3(\theta - \varphi)) \tag{18}$$

When the phase shift angle φ is equal to $\pi/4$ then (18) can be simplified to:

$$i_D(\theta) = I_{DC}(1 - \frac{\zeta_1}{\sqrt{2}}\cos\theta - \frac{\zeta_1}{\sqrt{2}}\sin\theta + \zeta_2 \sin 2\theta + \frac{\zeta_3}{\sqrt{2}}\cos 3\theta - \frac{\zeta_3}{\sqrt{2}}\sin 3\theta) \tag{19}$$

By introducing an empirical factor, γ, the above equation can be re-written as:

$$i_D(\theta) = I_{DC}(1 - \frac{\zeta_1}{\sqrt{2}}\cos\theta - \gamma\frac{\zeta_1}{\sqrt{2}}\sin\theta + \gamma\zeta_2 \sin 2\theta + \frac{\zeta_3}{\sqrt{2}}\cos 3\theta - \gamma\frac{\zeta_3}{\sqrt{2}}\sin 3\theta) \tag{20}$$

For the case when $\gamma = 0$, the above relation reduces to:

$$i_D(\theta) = I_{DC}(1 - \frac{\zeta_1}{\sqrt{2}}\cos\theta + \frac{\zeta_3}{\sqrt{2}}\cos 3\theta) \tag{21}$$

The maximum current I_{max} in (21) can be shown equal to $2I_{DC}$, hence (20) is rearranged as:

$$i_D(\theta) = I_{\max}(\frac{1}{2} - \frac{\zeta_1}{2\sqrt{2}}\cos\theta - \gamma\frac{\zeta_1}{2\sqrt{2}}\sin\theta + \gamma\frac{\zeta_2}{2}\sin 2\theta + \frac{\zeta_3}{2\sqrt{2}}\cos 3\theta - \gamma\frac{\zeta_3}{2\sqrt{2}}\sin 3\theta) \tag{22}$$

A plot for the drain current waveforms, normalized to I_{max}, for three different values of γ is presented in Fig. 3 showing symmetrical signals. The peak drain current is equal to 1.86 I_{max} when $\gamma = \pm 1$.

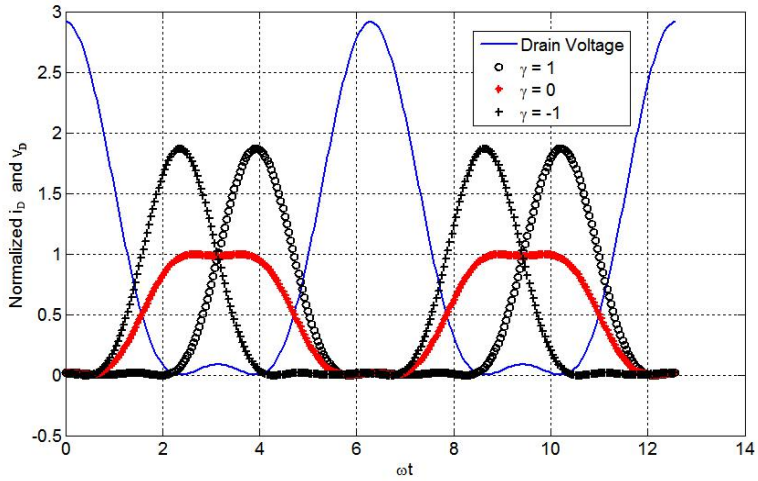

Fig. 3. Drain current waveforms with 2nd and 3rd harmonic tuning.

The drain current harmonic components are thus given by:

$$I_{d1} = (-\frac{\zeta_1}{2\sqrt{2}} + j\gamma\frac{\zeta_1}{2\sqrt{2}})I_{\max} \tag{23}$$

$$I_{d2} = -j\gamma\frac{\zeta_2}{2}I_{\max} \tag{24}$$

$$I_{d3} = (\frac{\zeta_3}{2\sqrt{2}} + j\gamma\frac{\zeta_3}{2\sqrt{2}})I_{\max} \tag{25}$$

The harmonic load admittances at the intrinsic current generator plane are therefore:

$$Y_{d1} = \frac{\zeta_1}{2}G_{opt} - j\gamma\frac{\zeta_1}{2}G_{opt} \tag{26}$$

$$Y_{d2} = j2\gamma\zeta_2 G_{opt} \tag{27}$$

$$Y_{d3} = \infty \tag{28}$$

The DC input power can be formulated as:

$$P_{DC} = \frac{1}{2} V_{DD} I_{\max} \tag{29}$$

On the other hand, the output RF power is evaluated from (8) and (23):

$$P_{out} = \frac{1}{4} \zeta_1 V_{DD} I_{\max} \tag{30}$$

The drain efficiency is found by dividing (30) by (29) so that it equals to $\zeta_1/2$ or 81%, with $\zeta_1 = 1.62$.

B. Drain Current with Semi-Square Waveform

In the previous mathematical models of the drain current signal, it was assumed that $i_D(\theta) \geq 0$. However, in computer simulations and practical circuit implementations the drain current waveform has some negative excursions resulting from the phase mismatches of the harmonic components caused by the nonlinearity of the active power device. Thus, a truncated square wave with the first three harmonics can be a suitable representation. In this case, the drain current waveform can be formulated as:

$$i_D(\theta) = I_{\max}\left(\frac{1}{2} - \frac{2}{\pi}\cos\theta + \frac{2}{3\pi}\cos 3\theta\right) \tag{31}$$

A family of waveforms can be generated by multiplying the above equation with a shaping term:

$$i_D(\theta) = I_{\max}\left(\frac{1}{2} - \frac{2}{\pi}\cos\theta + \frac{2}{3\pi}\cos 3\theta\right).(1 - \gamma \sin\theta) \tag{32}$$

After re-arrangement, the first three harmonic current components are:

$$I_{d1} = \left(-\frac{2}{\pi} + j\frac{\gamma}{2}\right) I_{\max} \tag{33}$$

$$I_{d2} = -j\frac{4\gamma}{3\pi} I_{\max} \tag{34}$$

$$I_{d3} = \frac{2}{3\pi} I_{\max} \tag{35}$$

A sketch of the drain voltage waveform normalized to V_{DD} and the drain current waveform normalized to I_{max} for three values of the parameter γ is depicted in Fig. 4. The peak value of drain current for $\gamma = \pm 1$ is 1.95 I_{max}.

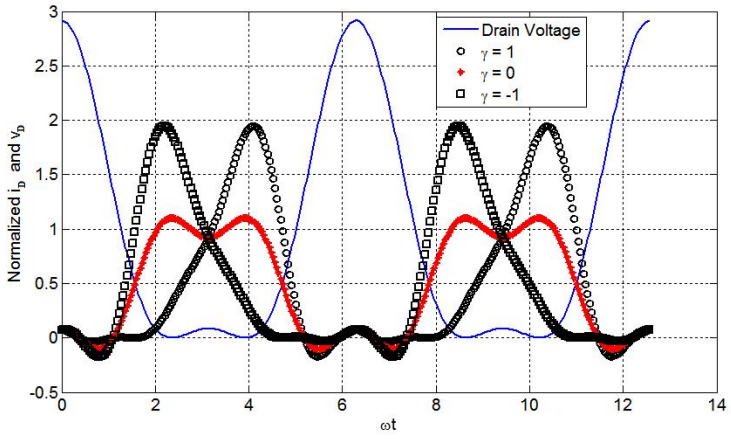

Fig. 4. Modified drain current waveforms with negative excursions.

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Consequently, the harmonic load admittances at the current generator plane are given by:

$$Y_{d1} = \frac{2\sqrt{2}}{\pi} G_{opt} + j\frac{\gamma}{\sqrt{2}} G_{opt} \tag{36}$$

$$Y_{d2} = -j\frac{16\gamma}{3\pi} G_{opt} \tag{37}$$

$$Y_{d3} = \infty \tag{38}$$

The DC input power is found from multiplying the DC components of drain voltage and current:

$$P_{DC} = \frac{1}{2} V_{DD} I_{\max} \tag{39}$$

The theoretical output RF power is calculated from (8) and (33):

$$P_{out} = \frac{\sqrt{2}}{\pi} V_{DD} I_{\max} \tag{40}$$

Finally, the DC to RF efficiency is given from (40) and (39) to be $2\sqrt{2}/\pi$, or 90%.

A comparison for the mentioned modes is clarified in Table I below in terms of the drain peak current and drain efficiency. It can be shown that the semi-square current waveform provides the highest theoretical drain efficiency (η_D) but at the expense of higher peak current due to the maximization of the fundamental component. Although the drain current waveform with 2nd and 3rd harmonic tuning provides comparable efficiency to that of the conventional case, but the harmonic components of the drain current are different as predicted in (23), (24), and (25). This gives slightly different shapes for the current signal patterns and load admittances. Besides, the third harmonic drain current component in (25) contains both real and imaginary parts and thereby provides more flexibility and wider design space in adjusting the third harmonic load admittance in case of the existence of a third harmonic drain voltage component in non-ideal realistic situations. This issue requires additional future analysis.

TABLE I. PERFORMANCE COMPARISON FOR THE THREE KINDS OF CURRENT WAVEFORMS.

Mode	$i_{D(peak)}$	η_D **(%)**
Conventional	1.68 I_{max}	81.65
2nd and 3rd harmonic tuning	1.86 I_{max}	81
Semi-square	1.95 I_{max}	90

IV. DESIGN OF A CICF POWER AMPLIFIER CIRCUIT

In order to confirm the theoretical analysis, a typical power amplifier circuit is to be designed and implemented to operate at the frequency range 800 – 1000 MHz. The RF power GaN HEMT CGH40006P has been selected for this design. It can provide 6 W output RF power with more than 12 dB power gain when operated from 28 V drain supply. It has a drain to source breakdown voltage of 120 V. In this design, the semi-square mathematical model for the drain current is adopted in the analysis to obtain higher theoretical drain efficiency.

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A. Device Characterization

The parasitic elements of the GaN HEMT can be evaluated from comparing the *S*-parameters of the packaged device (CGH40006P) with its bare chip model (CGH60008D) embedded with these elements by means of a circuit simulation program such as ADS of Keysight over a specified range of frequencies. The optimized values of the parasitic components are presented in Fig. 5 where the packaged model is composed of the intrinsic nonlinear model plus the parasitic components.

The output capacitance of the GaN HEMT can be assumed linear with acceptable results to simplify the analysis [14]. Based on this assumption, the harmonic load admittances at the extrinsic drain can be evaluated by linearly embedding the drain parasitic elements with the intrinsic admittances. The harmonic admittances at the current generator plane obtained from (36), (37), and (38) together with their counterparts at the package plane are sketched on an admittance Smith chart as depicted in Fig. 6 at a frequency of 900 MHz and R_{opt} of 90 Ω. This value of R_{opt} implies that I_{max} = 0.62 A, and $i_{D(\text{peak})}$ = 1.2 A. It can be seen from this sketch the effect of the parasitic elements in shifting the load admittances on the Smith chart in counter clockwise direction for the three harmonic admittances.

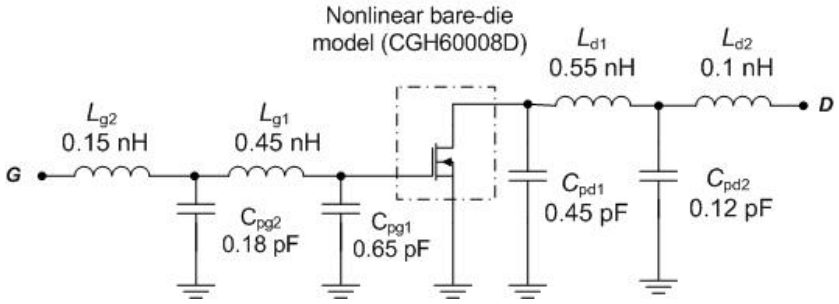

Fig. 5. Packaged model of the CGH40006P GaN HEMT.

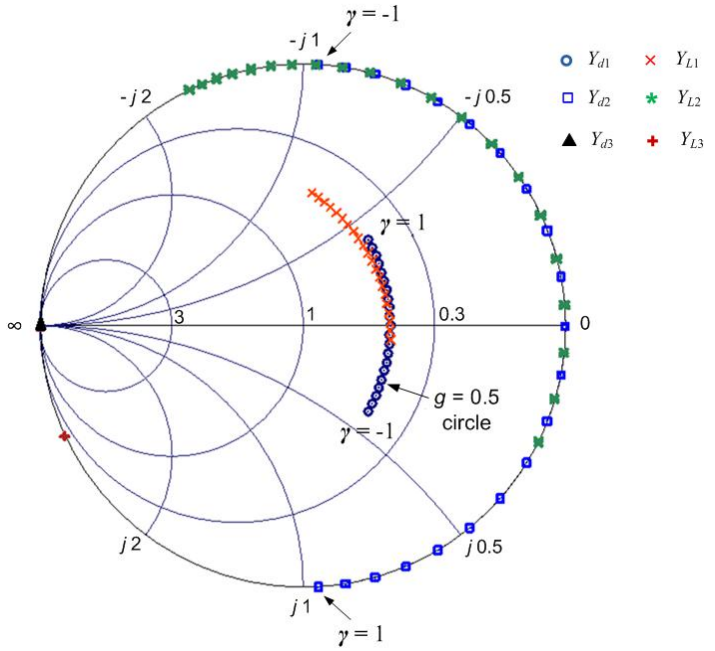

Fig. 6. Locus of the drain harmonic admittances at the current generator and package planes.

B. Performance Investigation

In order to evaluate the performance of the continuous inverse class F (CICF) power amplifier with the suggested drain current waveform, a computerized test setup has been suggested by means of the Keysight's ADS software and using the harmonic balance simulator. The proposed setup is presented in Fig. 7. In this schematic diagram, the intrinsic model of the power HEMT is utilized to view the intrinsic drain voltage and current signals properly. The source impedance Z_s can be adjusted to present the complex conjugate of the input large signal impedance at the specified signal level and frequency. The transistor is biased in class-AB at a drain voltage of 28 V and gate voltage of -2.7 V that produces a drain quiescent current of 130 mA. Biasing the active device with a considerable quiescent current has been shown to provide better efficiency and power gain performance in inverse class-F power amplifiers than biasing it at the threshold point [15]. An input power level of 25 dBm is chosen to drive the active device into the saturation region at a frequency of 900 MHz.

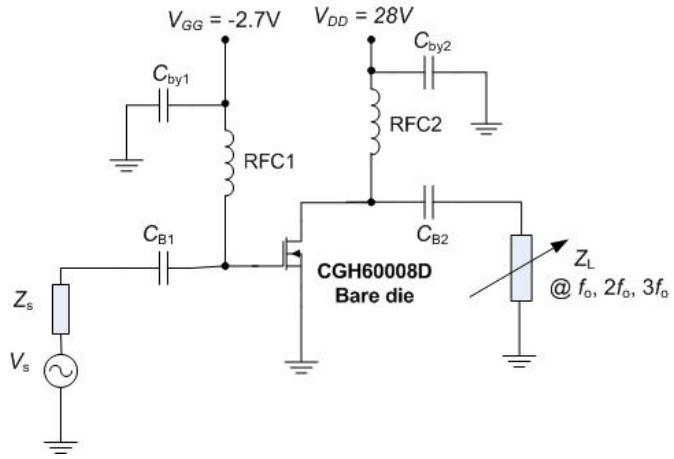

Fig. 7. Test circuit for amplifier characterization.

The intrinsic nonlinear model of the power HEMT, CGH60008D, includes the drain to source capacitance, C_{ds}, which should be taken into account. Therefore, the harmonic load impedances derived in (36), (37), and (38) should be modified to embed the output capacitance of the bare-chip model. The resulting harmonic impedances are used to terminate the bare die device model as depicted in Fig. 7. The real and imaginary parts of the fundamental harmonic load impedance $Z_{L1} = R_{L1} + jX_{L1}$ are given by:

$$R_{L1} = \frac{R_{opt}'}{1+(\gamma.\pi/4+\omega_0 C_{ds} R_{opt}')^2} \tag{41}$$

$$X_{L1} = \frac{R_{opt}'.(\gamma.\pi/4+\omega C_{ds} R_{opt}')}{1+(\gamma.\pi/4+\omega_0 C_{ds} R_{opt}')^2} \tag{42}$$

where:

$$R_{opt}' = \frac{\pi}{2\sqrt{2}} R_{opt} \tag{43}$$

The second harmonic load impedance becomes:

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$$Z_{L2} = j\frac{3\pi R_{opt}}{6\pi\omega_0 R_{opt} C_{ds} - 16\gamma} \tag{44}$$

On the other hand, the third harmonic load impedance is:

$$Z_{L3} = 0 \tag{45}$$

The current flowing into the virtual drain terminal D' in Fig. 1 (i_D') represents the current measured using the harmonic balance simulator. The drain current at the current generator plane is found from:

$$i_D(t) = i_D'(t) - C_{ds}\frac{dv_D(t)}{dt} \tag{46}$$

where C_{ds} is found to be 0.64 pF [16], knowing that (46) is evaluated using the ADS capabilities.

The drain current and voltage waveforms at the current generator plane are presented in Fig. 8 for three different values of the parameter γ. These waveforms are consistent with the theoretical signals sketched in Fig. 4. The simulated drain voltage waveform has a half sinusoidal shape with a peak value of 82 V which resembles the theoretically predicted value in (1). The drain current waveforms have some negative excursions similar to the theoretical signals presented in Fig. 4 with peak values of 1.25A when $\gamma = \pm 1$, which is very close to the estimated theoretical value as previously illustrated in section IV-A where the calculated value of I_{max} = 0.62 A and that of $i_{D(peak)}$ = 1.2 A. Likewise, the drain current has a semi-square wave shape for γ = 0 with a peak value of 0.7 A. The noted small deviation in the simulated current signals shown in Fig. 8 from the theoretically suggested waveforms in Fig.4 is referred to the nonlinearities presented in the HEMT CAD model, especially the gate to source and gate to drain intrinsic capacitances that are voltage dependent. These nonlinearities can generate some additional harmonics in the drain current signal.

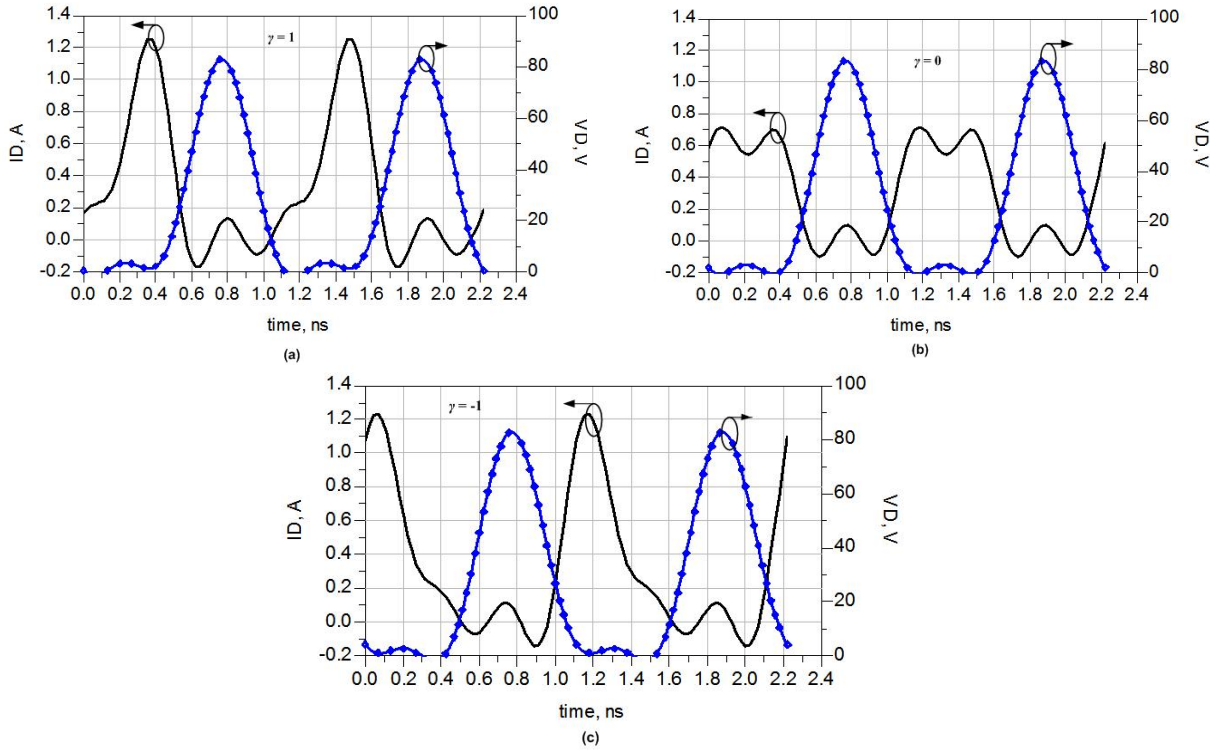

Fig. 8. Intrinsic drain voltage and current waveforms for γ = 1 (a), γ = 0 (b) and γ = -1 (c).

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The simulated drain efficiency against the empirical parameter γ is shown in Fig. 9. In this sketch, it appears that the simulated efficiency is approximately maintained constant and *varies* from 87% to 90% for various values of γ. On the other hand, the simulated large-signal power gain and output RF power are found to be constant at 14 dB and 39 dBm respectively over the same range of γ.

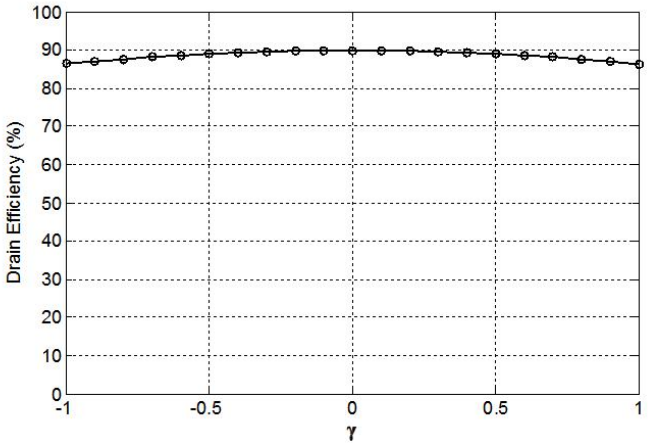

Fig. 9. Simulated drain efficiency versus γ.

C. Design of Matching Networks

The output matching (or load) network can be synthesized by evaluating the harmonic load impedances at the package plane for the desired frequency band. These impedances can be calculated at the intrinsic current generator plane from (36) through (38) and then be transformed into the package plane after embedding the parasitic elements at the drain of the HEMT. In order to synthesize realizable load network, the harmonic load impedances should move in clockwise direction on the Smith chart with the increase in frequency. Therefore, the parameter γ can be selected in ascending order with the increase in frequency when calculating the load impedances.

For a specified number of selected sample frequencies, n, within the frequency band of interest, the step size in frequency can be calculated from:

$$\Delta f = \frac{f_H - f_L}{n} \tag{47}$$

where f_H is the upper band frequency and is equal to 1 GHz, and f_L is the lower band frequency and is equal 800 MHz. If n is selected to be 10, then $\Delta f = 20$ MHz.

Similarly, an increment in the parameter γ can be evaluated from:

$$\Delta\gamma = \frac{\gamma_{\max} - \gamma_{\min}}{n} \tag{48}$$

When $\gamma_{\min} = 0.6$ at 800 MHz and $\gamma_{\max} = 1$ at 1 GHz, then $\Delta\gamma = 0.04$. At each sample frequency in the band, a corresponding value of γ is found as $\gamma_i = \gamma_{i-1} + \Delta\gamma$. Based on this approach, the drain harmonic impedances are evaluated from (36), (37) and (38) and then transformed into the package reference plane after linearly embedding the package components. The selection of $\gamma = 0.6$ at the lower band edge is necessary to avoid very high peak drain current that may exceed the maximum allowable device value as predicted from (32). The range over which γ changes is dependent on the desired

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bandwidth. The evaluated optimum harmonic load impedances across the required frequency band are sketched on the Smith chart shown in Fig. 10.

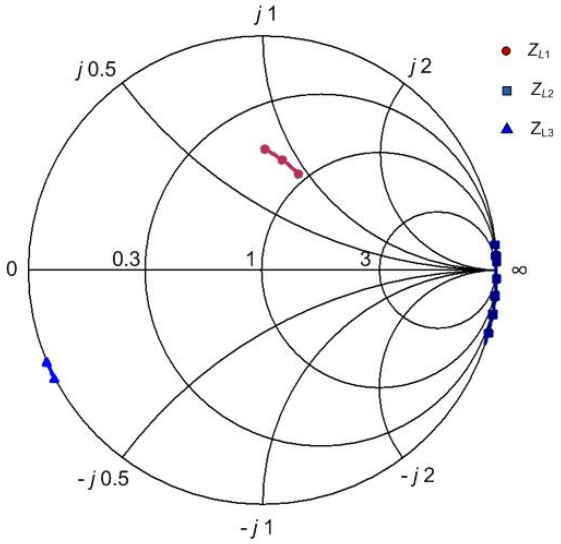

Fig. 10. Estimated normalized harmonic load impedances.

A typical output matching circuit consisting of three low-pass L-sections has been designed and optimized to fit the targeted harmonic impedances of Fig. 10. The structure of this network is depicted in Fig. 11 where it is implemented as microstrip lines on Rogers RO4350B substrate. The impedance response of the optimized load network is presented on the Smith chart of Fig. 12, showing a close behavior to the computed response depicted in Fig. 10.

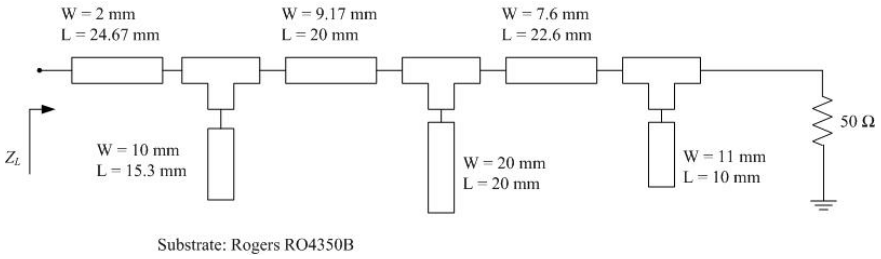

Fig. 11. Optimized microstrip load network for the power amplifier.

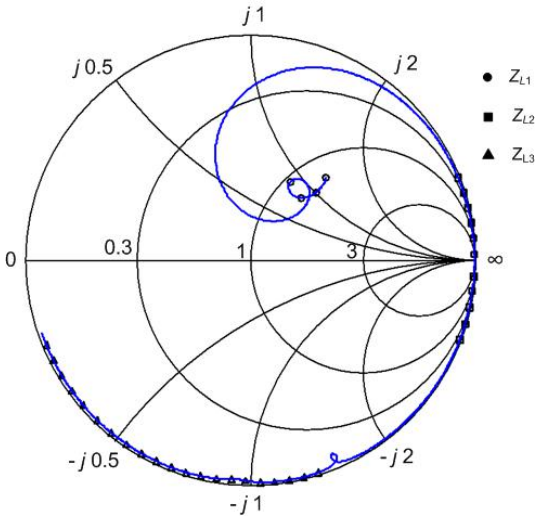

Fig. 12. Simulated impedance response of the optimized load network.

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The load network has been inserted at the output port of the power device and the circuit has then be simulated by means of the non-linear large signal *S*-parameter test provided by the Keysight ADS simulator at the specified power level and frequency range to check the stability factor. An *RC* network was inserted at the input port to increase the stability factor and prevent any tendency into low frequency oscillation. With the stability circuit presented at the input port, the amplifier circuit was simulated to extract the large signal input impedance across the entire band. The input matching network was designed to transform the device's input impedance into 50 Ω and thereby to increase the power gain and achieve minimum reflected power. The final schematic of the designed power amplifier circuit is sketched in Fig.13, where two RF chokes are utilized to isolate the RF circuit from the drain and gate DC supplies while providing the necessary DC current and bias voltages.

D. Simulation Results

The amplifier circuit has been simulated by means of the harmonic balance algorithm that is integrated with the ADS software. The intrinsic drain voltage and current waveforms at the current generator plane of the power HEMT are displayed in Fig. 14 for three simulation frequencies at 800, 900, and 1000 MHz respectively.

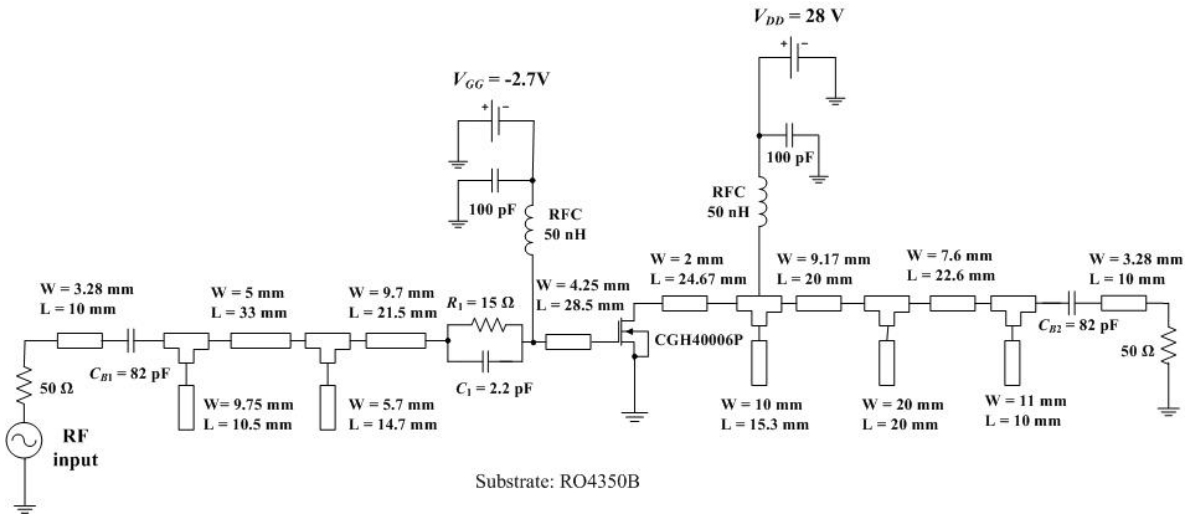

Fig. 13. Schematic diagram of the designed RF power amplifier.

At the lower band edge, the peak amplitude of the drain current waveform is the lowest amongst the three simulation frequencies taking a value of 0.65 A approximately. At the center frequency of the band the peak current values increases to 0.9 A, while it reaches to about 1.1 A at the upper band edge. The drain voltage waveforms, on the other hand, have an approximate half sinusoidal shape with very small third harmonic component. These waveforms are consistent with the theoretical patterns presented in Figure 4 where, in this case, it is assumed that γ = 0.6 at 800 MHz, γ = 0.8 at 900 MHz and γ = 1 at 1 GHz. It is also noted that the drain current waveform possesses some negative part as predicted by (32) and Fig. 4. Some additional higher order harmonics in the drain current are noted as a result of the power transistor's nonlinearity and the deviation between the theoretically estimated load impedances in Fig. 10 and the actual simulated values presented in Fig. 12.

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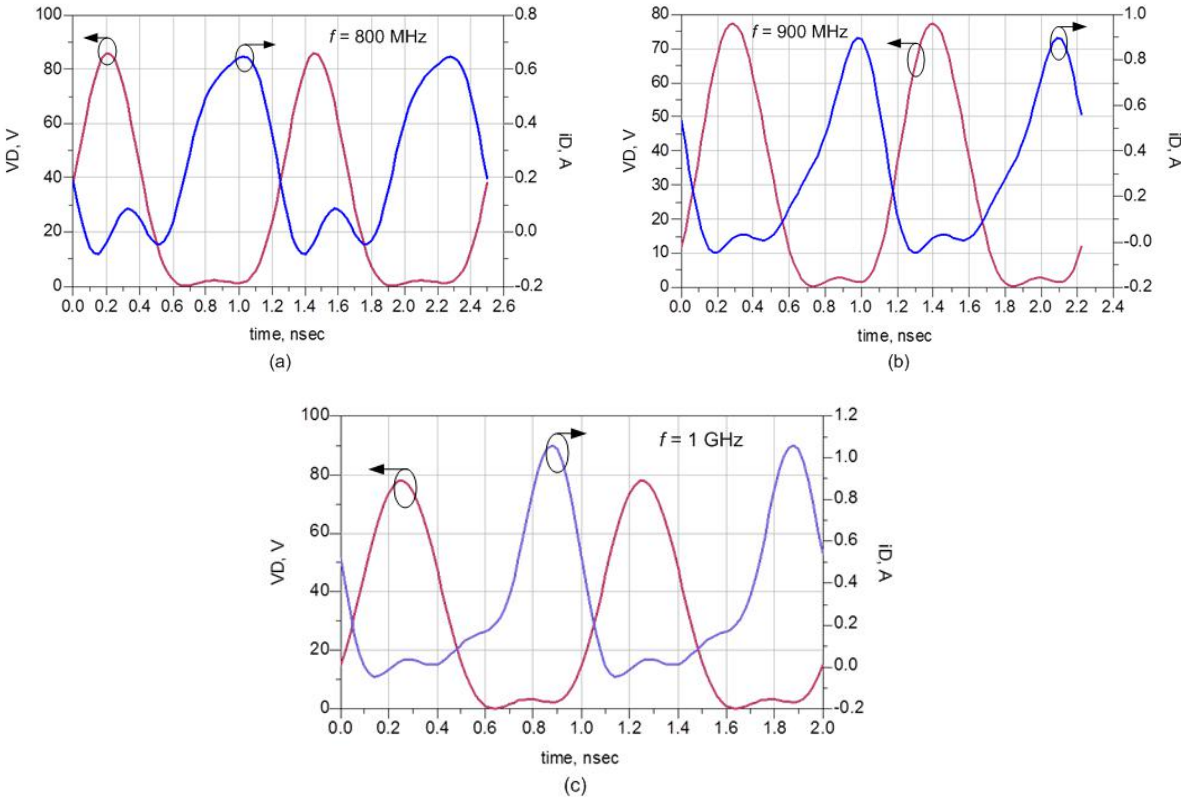

Fig. 14. Simulated drain voltage and current waveforms of the power amplifier.

The performance parameters of the circuit, such as drain efficiency, power-added efficiency, output RF power, and power gain are swept against input RF power level in Fig. 15 at the center frequency of the desired band. It can be shown that the small signal power gain is around 22 dB but it is compressed to 13.7 dB at a nominal input drive power of 25 dBm. The relatively high input drive level is necessary to drive the power GaN HEMT deeply into the nonlinear region to generate the harmonics that are necessary to shape the drain voltage and current waveforms for maximized drain efficiency. The saturated output power is about 38.7 dBm at an input power of 25 dBm while the power-added efficiency is about 80.4 % and starts to drop thereafter due gain compression. At this power level, the DC-to-RF efficiency is about 83.8 %.

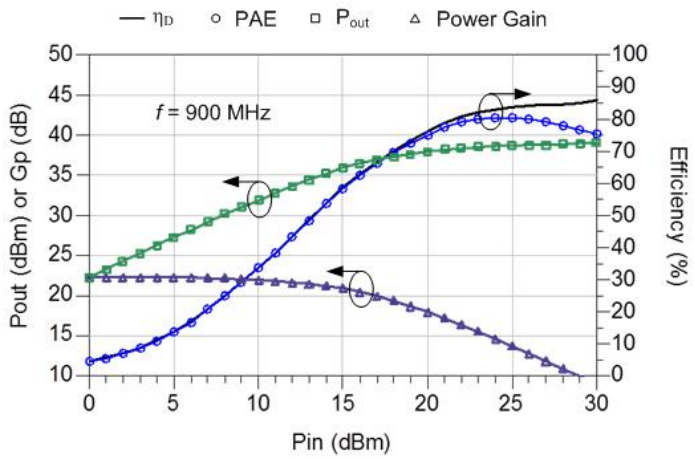

Fig. 15. Power amplifier performance parameters versus input drive power at 900 MHz.

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In Fig. 16, the same amplifier performance characteristics are simulated versus frequency for the band of interest with an input power of 25 dBm. It can be seen that the drain efficiency varies between 82% and 86%, revealing efficient operation across the desired band. On the other hand, the large signal power gain seems to be flat and it is actually deviating around 13.5 ± 0.2 dB, while the output RF power is about 38.5 dBm. The drain efficiency can slightly be increased to approach the predicted theoretical limit of 90% by further increase in the input RF power but at the expense of more compression in power gain and reduction of the power-added efficiency (PAE). Finally, the input return-loss and output second harmonic distortion are sketched in Fig. 17 against frequency. The input return loss is below -15 dB, showing an acceptable impedance matching and low reflected power at the input port of the power amplifier across the desired band. The second harmonic distortion at the output of the power amplifier is reduced to values below -30 dBc over the entire frequency band by the filtering action of the output matching network. An improvement in the second harmonic distortion reduction is noted at higher frequencies within the band because the attenuation of the output filter increases at higher frequencies. Although harmonically tuned power amplifiers are adequate for constant envelope waveforms such as the GSM signal but linearization techniques are very necessary for amplifying variable envelope signals that have large peak to average power ratio like the OFDM signal to improve the adjacent channel power ratio (ACPR) at the expense of some loss in efficiency.

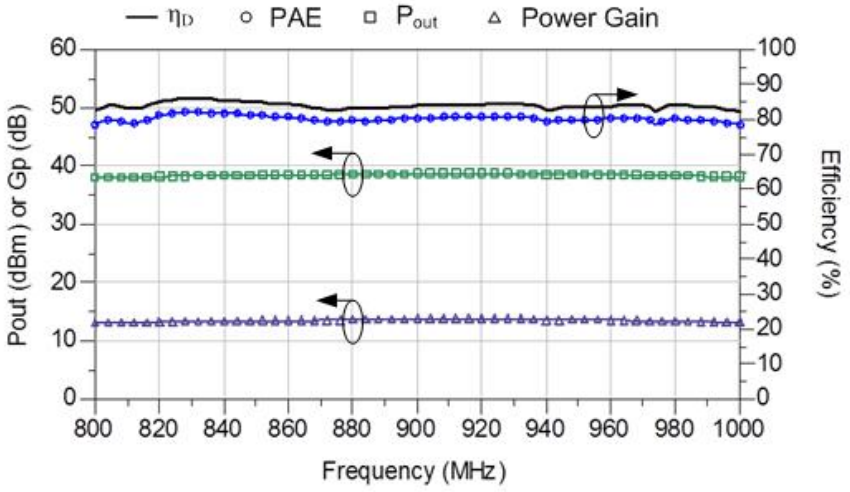

Fig. 16. Simulated amplifier characteristics versus frequency.

A comparison between the performance parameters of the designed circuit with some other recent works on continuous inverse class-F power amplifiers is presented in Table II, revealing a competitive efficient operation although some degradation in the response is expected if the circuit is practically implemented due to additional parasitics and the deviation between the transistor CAD model and its actual physical behavior. Nevertheless, the simulation results can give a close picture for any future implementation.

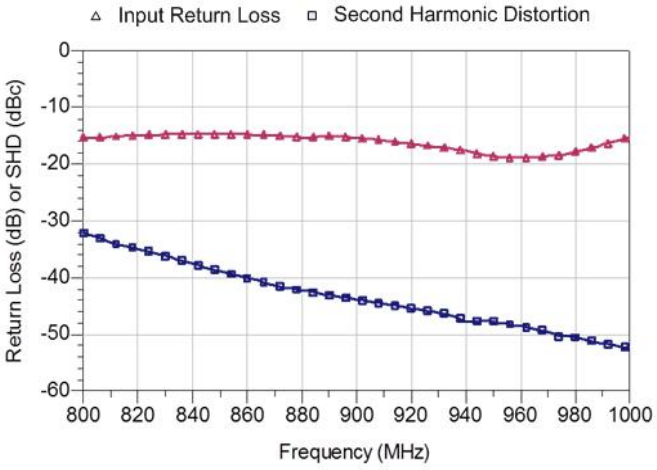

Fig. 17. Input return loss and second harmonic distortion versus frequency.

TABLE II. COMPARISON WITH OTHER RECENT WORKS ON CICF PAS.

Reference	Frequency Range (GHz)	Drain Efficiency (%)	Power Gain (dB)	RF Power (dBm)
[9]	1.35 – 2.5	68 - 82	15.2 – 17	40.97 - 42.55
[10]	2.1 – 2.4	72 - 84	10.4-13.3	39.7 – 40.8
[17]	2.5 – 4.1	47 - 75	8 – 14	39.59 – 42.64
[18]	1.35 – 2.35	71 - 82	10.1 – 11.5	40.1 – 41.5
This work	0.8 – 1	82 - 86	13.3 – 13.7	38.3 – 38.7

V. CONCLUSION

A methodology for analyzing continuous inverse class F RF power amplifiers with new drain current waveform characterization has been presented and confirmed. It has been found that a theoretical drain efficiency of 90% can be obtained with such waveform, thereby giving more accurate prediction of the amplifier performance. Furthermore, a simplified analytic method for estimating the optimum harmonic load impedances at the device's package plane across the desired frequency range has been clarified. To verify the presented approach, a typical CICF power amplifier circuit has been designed and simulated successfully to operate at the GSM band from 800 to 1000 MHz. The simulation results show satisfactory performance prediction based on the developed theory. However, in order to validate the methodology presented in this work practically a prototype microstrip power amplifier model can be constructed and tested based on the schematic diagram presented in Fig. 13. A main limitation for this approach is that the device required fundamental and harmonic load impedances have been calculated from the derived equations rather than from extensive measurements using either the nonlinear embedding technique or the load-pull test. But this closer estimation of the harmonic load impedances can simplify and accelerate the load-pull test in case of carrying out it practically.

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