A CMOS UWB Transmitter with Vivaldi Array for Ultra-fast Beam steering Microwave Radar

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***Abstract*— This work presents a new Ultra Wide Band (UWB) beamforming fifth-order derivative Gaussian pulse transmitter with dual small Vivaldi antennas for remote acquisition of vital signals in impulse radar applications. The system consists of a programmable delay circuit (PDC or τ), a UWB pulse generator (PG) circuit and an array of two Vivaldi planar antennas. The circuits is designed using the 0.18µm CMOS IBM process. Spice simulations show the pulse generation with 90mVpp amplitude and 300ps width. The average power consumption is 120µW per pulse, using a 2V power supply at a pulse repetition rate (PRR) of 100MHz. Full tridimensional electromagnetic simulations, using CST MWS, show the main lobe radiation with a gain of 5.5dB, and a beam steering between 20º and -17.5º for azimuthal (θ) angles at the center frequency of 7.5GHz.**

***Index Terms*—** Health monitoring; respiration rate; beamforming; phased array; vital signals; heartbeat signals.

I. INTRODUCTION

Considerable effort has been focused on the generation and transmission of UWB pulses, which can be used in a wide range of applications, such as in the remote acquisition of heartbeat signals of workers in an industrial plant, the measurement of respiration rate of soldiers in a military vehicle, or to track victims in landslide rubble [1-3]. This system consists of a transmitter, described in this work, and a receiver to perform telemetry for estimating the vital signs through detection of heart and lungs.

In order to acquire those signals, it is required to have a high precision system that can dynamically capture the signals of each individual on its fixed position, since this analysis in motion can cause significant changes in the shape of the UWB waveform [4].

If the spectral power of the UWB pulses is spread along an ultra-wide frequency range, the interference with other communication systems, such as phones, GPS systems, Bluetooth, and W-LAN IEEE 802.11, could be minimized [5]. A critical point is that reflections from the environment need to be minimized, in order to preserve the pulse shape and facilitate the detection process. Therefore, it is essential to use a radar system equipped with high-gain directional antennas [4]. The proposed arrangement, based on the model discussed in ref. [1], contains a timed-array transmitter system which is equipped with an antenna array that allows beam steering (Fig. 1). In the figures 1(c) and 1(d), two polar gain plots are shown, where each one corresponds to a determined delay set configured according the 1-byte word sent to the PDC circuit, shown in Fig. 1(a).

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This paper is organized as follows: Sec II presents the transmitter circuit and antenna array architecture and design; the integrated system post-layout Spice simulations with MicroWind 3[6] combined with LTSpice 4[7] for layout and schematic, where effects of crosstalk coupling vertical and horizontal, input noise and parameters variation by Monte Carlo were considered during the Spice simulations. Section III presents the results of electromagnetic propagation simulation in CST MW 2011[8], together with the results of Spice simulations, while Section IV presents the conclusions.

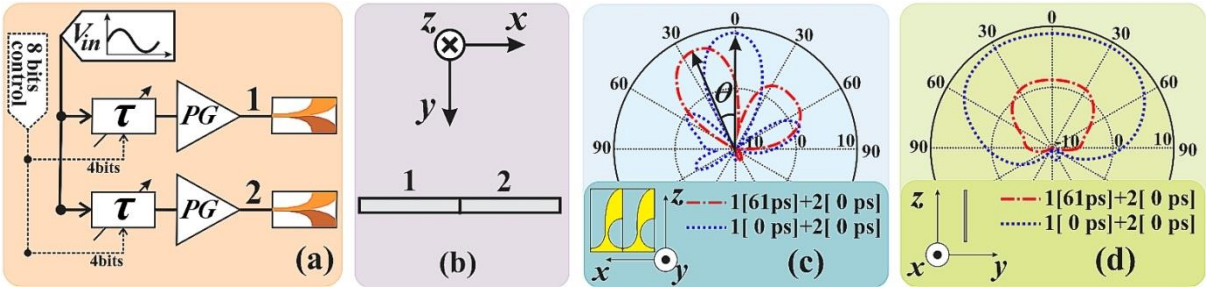

Fig. 1 - UWB Beamforming Transmitter. (a) A general structure of beamforming; (b) Back view of the two antenna array; alongside with the axes orientation; (c) array gain pattern in the azimuth plane and antenna array view from the top; (d) array gain pattern in the elevation plane and lateral antenna array view.

II. TIMED-ARRAY TRANSMITTER CIRCUIT AND ANTENNA ARRAY WITH BEAMFORMING CAPABILITY

Radar systems based on timed or phased antenna have several advantages in comparison to mechanically scanned systems, since with electronic configurations the beam steering can be achieved rapidly without the use of complicated mechanical systems [9], e.g. when the antennas are excited with a delay time of 61ps and 0ps for channels 1 and 2 respectively, the same channels will vary the azimuthal angle (θ), as seen in Fig. 1(c), and elevation angle (φ) as seen in Fig. 1(d). Each block of the transmitter is explained, including the antenna array in the next sections.

A. Programmable delay array – PDC

The proposed PDC is shown in Fig. 2(a). The circuit consists of two independent channels (such that each antenna can be independently fed), further details shown in Fig. 2(b), and each one is formed by two buffers formed by two static inverters (Fig. 2(e)), connected in series with a digital variable capacitor (Fig. 2(c)), between the signal line and Vss.

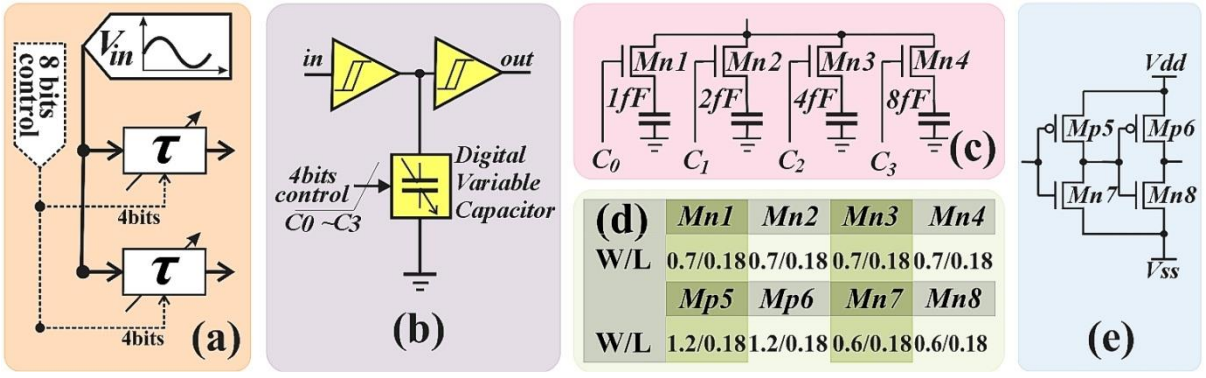

Fig. 2 - General PDC array structure: (a) PDC array; (b) PDC Unit; (c) Digital Variable Capacitor Circuit; (d) MOS dimension table of the PDC Unit; (e) Buffer Circuit.

The variable capacitor charging and discharging periods modify the properties of transition time

between the two internal buffers, therefore providing a controlled delay.

B. The 5th derivative Gaussian pulse generator

UWB radars can be used as a tool for analysis of human vital signs in a noninvasive form. They are not influenced by clothing or other covers and can be used at range of several meters [10].

The first consideration before designing a UWB pulse generator is to select the type of pulse that meets certain conditions [11]. According to refs. [11, 12], the Gaussian pulse can be expressed as,

$$g_{(t)} = \frac{A}{\sqrt{2\pi}\sigma} e^{\left(-\frac{t^2}{2\sigma^2}\right)} \tag{1}$$

where $\boldsymbol{\sigma}$ is the time variance and $\boldsymbol{A}$ is the pulse amplitude. The Gaussian pulse is a natural candidate for a UWB pulse because it has a wide bandwidth and no side lobes, albeit it contains a DC and lower frequency components, which cannot be transmitted by the antennas considered here.

The fifth-order derivative Gaussian pulse is one of the best choices, for noninvasively health monitoring, because it fully complies with the FCC mask for indoor applications [11-13] and there is no DC energy (zero frequency). As a result, the fifth-order derivative Gaussian was chosen for the proposed pulse generator development. Therefore, the proposed pulse generator is expressed as

$$g^{(5)}(t) = A\left(-\frac{t^5}{\sqrt{2\pi}\sigma^{11}} + \frac{10t^3}{\sqrt{2\pi}\sigma^{9}} - \frac{15t}{\sqrt{2\pi}\sigma^{7}}\right) e^{\left(-\frac{t^2}{2\sigma^2}\right)} \tag{2}$$

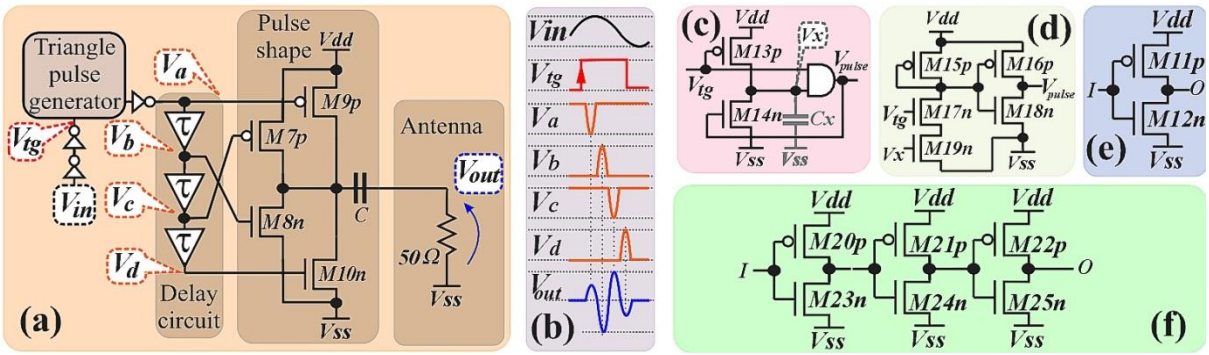

Fig. 3 – The proposed UWB 5th derivative Gaussian pulse generator: (a) General structure of the proposed pulse generator; (b) Simplified time diagram; (c) Pulse Generator proposed for [11]; (d) AND gate formed by a pseudo n-MOS NAND gate and a static inverter; (e) Static inverter circuit; (f) Three Inverter Delay Circuit.

The novel system architecture is illustrated in Fig. 3(a). It consists of two identical static inverters connected in series. They transform the arbitrary input signal $\boldsymbol{V_{in}}$ into a square waveform $\boldsymbol{V_{trigger}}$ ($\boldsymbol{V_{tg}}$). Next, there is a triangular pulse generator [14], responsible for the generation of a triangular pulse that is inverted by the static inverter ($\boldsymbol{V_a}$). This inverted triangular pulse is later spread and inverted by the delay line ($\boldsymbol{V_b}$, $\boldsymbol{V_c}$, and $\boldsymbol{V_d}$), each time the wave excites the pulse shape transistors (M9p, M8n, M7p, and M10n). The current that passes through the C capacitor blocks out the DC component, and also generates the $\boldsymbol{V_{out}}$ signal that is shaped according to the 5th derivative of the Gaussian pulse, as illustrated in Fig. 3(b).

Each subsystem of the pulse generator is further described:

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1) Square-wave rectifier

This subsystem consists of two identical static inverters used to rectify time-varying waveforms such as square waves, following the proposed pulse generator presented in [15]. The inverter architecture is illustrated in Fig. 3(e), which consists of the pMOS (M11p with w=4µm and l=0.2µm) and the nMOS (M12n with w=2µm and l=0.2µm) transistors, operating as switches. When the input signal has a low level (***Vss***), the nMOS gate is reversely biased while the pMOS gate is directly biased, therefore generating a high level (***Vdd***) at its output. Conversely, a high level signal is applied in the input generates a low level (***Vss***) on the output.

Because the average time response from Monte Carlos simulations of the proposed inverter lies in the range of 40ps (more than seven times faster compared to the transition from a sine wave of the same frequency), the connection of two inverters in series shapes the input time-varying signal into a square wave.

The Fig. 4 shows the waveforms V_{in}, and V_{in} inverted V_{tg} as a result of the Spice simulation [6, 7].

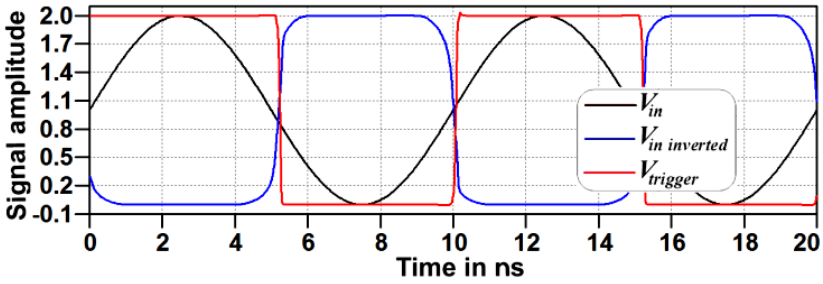

Fig. 4 - Waveform of the input signal (V_{in}) that passes through the first static inverter ($V_{in\ inverted}$) and ($V_{trigger}$), after it passes through the second static inverter.

The same inverter is used in the output of the triangular pulse generator.

2) Triangle pulse generator

The Triangle pulse generator used in this work is based in the developments of [14] and is the core of the 5th derivative Gaussian proposed pulse generator. Fig. 3(c) shows the triangle pulse generator, which is originally used as the single pulse generator [14], and was developed around a simple feedback network and an AND gate.

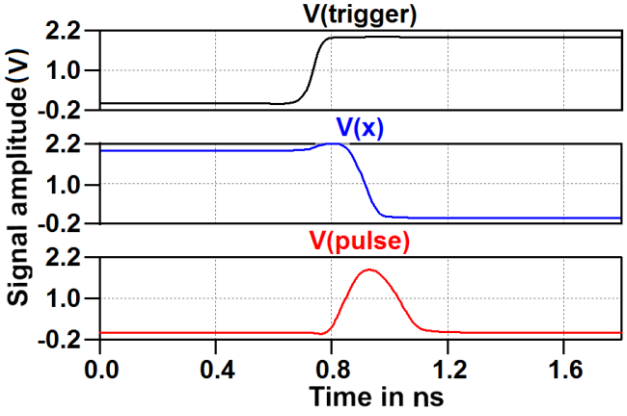

Fig. 5 - Waveform of the rectified input signal ($V_{trigger}$), the middle signal of triangle pulse generator (V_x) and the pulse generated (V_{pulse}).

The detailed architecture of the triangle pulse generator is shown in Fig. 3(c) and the detailed signal

flow is shown in Fig. 5. When $\boldsymbol{V_{trigger}}$ is held at a low level (***Vss***), the AND gate (Fig. 3 (d)) output is also at low level, thus the nMOS transistor M14n (with w=1µm and l=0.2µm) is off. The parasitic capacitor $\boldsymbol{C_x}$ is then charged to ***Vdd*** by the pMOS transistor M13p (with w=4µm and l=0.2µm). At the moment that the $\boldsymbol{V_{trigger}}$ signal reaches the high level (***Vdd***), M13p is immediately turned off and the AND gate output reaches a high level after a short gate delay $\boldsymbol{\tau_{AND}}$, therefore M14n is turned on to discharge the capacitor $\boldsymbol{C_x}$. When the signal $\boldsymbol{V_x}$ is changed to a level below the threshold voltage of the AND gate $\boldsymbol{V_{TH\ AND}}$, the AND gate output changes to a low level again after ***T***, thereby a triangular pulse ($\boldsymbol{V_{pulse}}$) is produced. Considering that the switch-on impedance of M14n is $\boldsymbol{R_{ON}}$, it can be estimated that:

$$V_x(t) = V_{dd} \times e^{-t/R_{ON}C_x} \tag{3}$$

when $\boldsymbol{V_x}(t)$ is changed to a level below $\boldsymbol{V_{TH\ AND}}$, the AND gate output is at low level and turns M14n off after the gate delay ($\boldsymbol{\tau_{AND}}$). The discharging time is:

$$\tau_D = R_{ON}C_x \ln\left(V_{dd}/V_{TH_{AND}}\right) \tag{4}$$

and the triangle pulse width ($\boldsymbol{\tau_{tp}}$) is equal to the sum of the $\boldsymbol{\tau_{AND}}$ time with (4):

$$\tau_{tp} = \tau_{AND} + \tau_D = \tau_{AND} + R_{ON}C_x \ln\left(V_{dd}/V_{TH_{AND}}\right) \tag{5}$$

Therefore, we conclude that the pulse width varies with the following characteristics:

- AND gate delay time ($\boldsymbol{\tau_{AND}}$);
- Parasitic capacitance of the interconnection x ($\boldsymbol{C_x}$);
- M14n switch-on impedance ($\boldsymbol{R_{ON}}$);

It should be stressed that $\boldsymbol{R_{ON}}$ is not constant, since $\boldsymbol{V_{pulse}}$ is variable. Further circuit simulations may be required to compute more accurate pulse widths.

3) Delay circuit

The delay unit is formed by three sets of identical static inverters. In Fig. 3(f), each implemented inverter consists of the nMOS and pMOS transistors, for the first inverter they are M23n (with w=2µm and l=0.2µm) and M20p (with w=4µm and l=0.2µm), respectively.

The delay time depends on the transistor channel dimensions; on the parasitic capacitances and the number of inverters in the delay line. This particular setting for the delay circuit was chosen due to its simplicity and compact topology. The outputs of the $\boldsymbol{V_{pulse}}$, $\boldsymbol{V_{shape1}}$ ($\boldsymbol{V_a}$) and the three delay elements are $\boldsymbol{V_{shape2}}$ ($\boldsymbol{V_b}$), $\boldsymbol{V_{shape3}}$ ($\boldsymbol{V_c}$), and $\boldsymbol{V_{shape4}}$ ($\boldsymbol{V_d}$), respectively, and they have an average width time of 190ps. Fig. 6 shows $\boldsymbol{V_{pulse}}$ and the other triangle waves that excite the transistors forming the pulse shaping stage.

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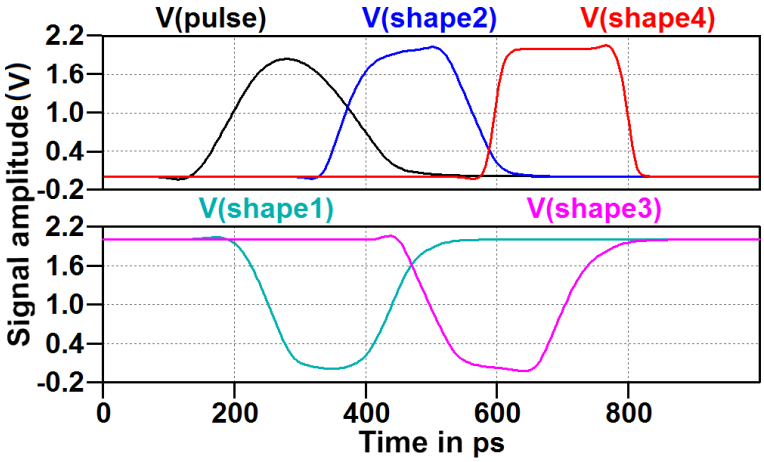

Fig. 6 - Waveform of the triangles pulses starting with the input V_{pulse} signal, followed by V_{shape1} (V_a), V_{shape2} (V_b), V_{shape3} (V_c), and V_{shape4} (V_d).

4) Pulse shaping stage

The development of the pulse shaping stage presented in this paper is based on [1, 11, 14, 15]. The pulse shaping stage implemented two charge-pumps, each consisting of two transistors, a pMOS and a nMOS, M9p (with w=2µm and l=0.2µm), M8n (with w=6µm and l=0.2µm), M7p (with w=6µm and l=0.2µm), and M10n (with w=2µm and l=0.2µm), as shown in Fig. 3(a). The charge-pump output currents are controlled and combined successively by these transistors; as a result, a fifth derivative Gaussian pulse is generated, illustrated in Fig. 3(b) and its waveform is shown in Fig. 8(a). The output pulse amplitude V_{out} is controlled by the charge-pumps output transistors. The transistor sizes are chosen based on the required amplification level to shape the output UWB waveform [10,14].

5) Pulse generator simulation results

The simulation of the proposed UWB pulse generator in post-layout Spice model shows that the circuit can be robustly operated, in other words, showing the 5th Gaussian pulse waveform at V_{out} unchanged with 20% variation of the parameters in Monte Carlo simulations. In order to confirm this, the circuit was simulated in several PRR's up to the GHz band range. The results from 100MHz up to 1.0GHz are shown in Fig. 7, where Fig. 7(a) shows the input sinusoidal signal waveform (V_{in}) and its rectified signal ($V_{trigger}$) at 100MHz. Fig. 7(b) presents the waveform of the pulse simulated (V_{out}) with a PRR of 100MHz, Fig. 7(c) shows the waveform V_{in} and $V_{trigger}$ at 500MHz. Fig. 7(d) shows the waveform V_{out} with a PRR of 500MHz, in the GHZ range finally, the Fig. 7(e) shows the wave form V_{in} and $V_{trigger}$ at 1.0GHz and Fig. 7(f) show the waveforms of V_{out} pulse train at PRR of 1.0GHz.

The simulation results showed that the fifth-order derivative Gaussian pulse is similar to the theoretical pulse calculated , as shown in Fig. 8(a). The amplitude of the simulated pulse is 90mVpp and its pulse width has 300ps. The average power consumption of 120µW per pulse is found at an input PRR's of 100MHz and 2V power supply.

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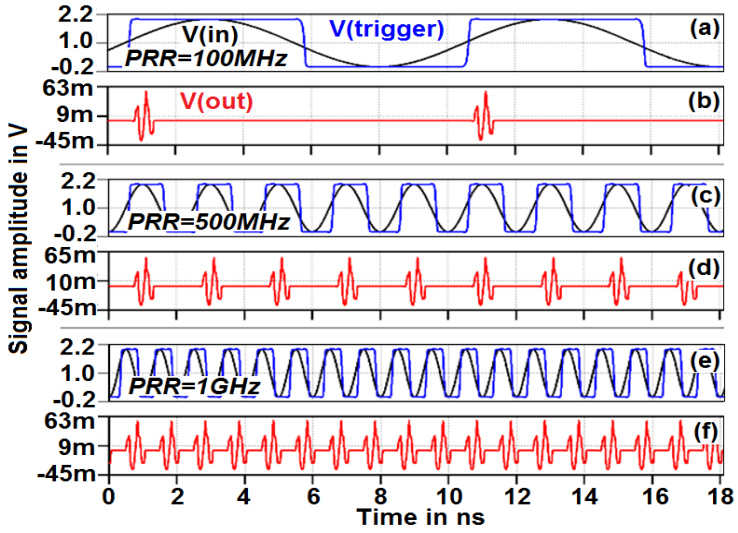

Fig. 7. Pulse simulated with different PRR: (a) V_{in} and $V_{trigger}$ at 100MHz. (b) V_{out} with PRR at 100MHz. (c) V_{in} and $V_{trigger}$ at 500MHz. (d) V_{out} with PRR at 500MHz. (e) V_{in} and $V_{trigger}$ at 1.0GHz. And (f) V_{out} with PRR at 1.0GHz.

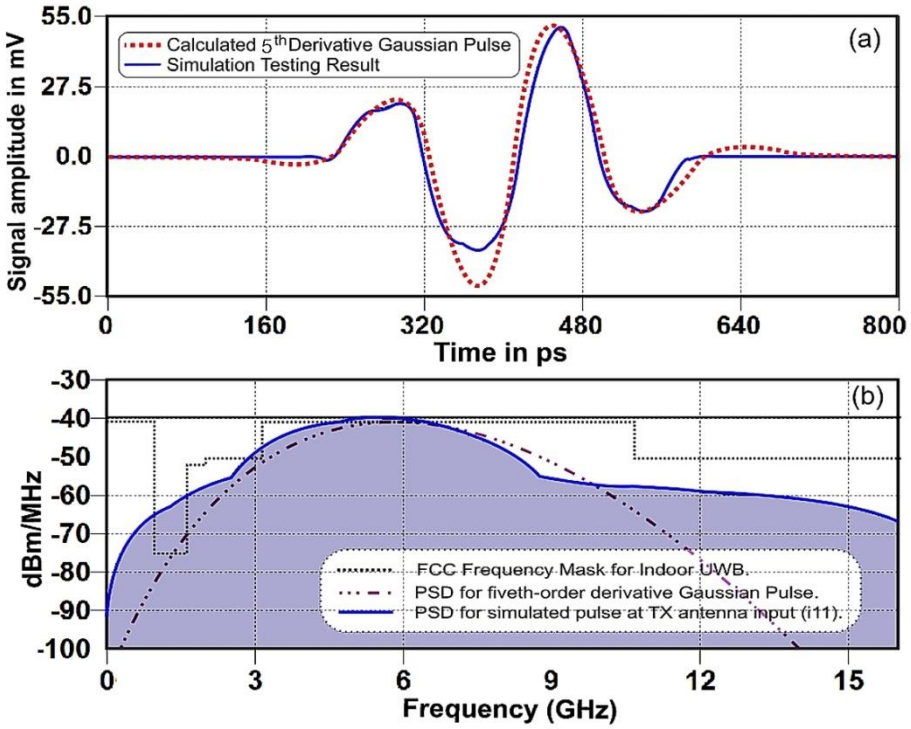

Fig. 8. (a) Simulated versus theoretical 5th Derivative Gaussian Pulse, (b) Spice Power Spectral Density of output pulse.

Figure 8(b) shows that the pulse spectral density is in good agreement with the FCC mask for UWB applications. The simulated power spectral density (PSD) of the proposed pulse is indicated in solid line, whereas the three-dot-dashed line shows the theoretical fifth-order Gaussian pulse PSD, alongside with the FCC mask for indoor UWB applications.

Table I compares this design with others reported in the literature. Comparison with [16] shows that the power consumption of this design is lower, as a result of the lower signal duration and smaller amplitude of the pulse, although the higher ***Vdd*** level.

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TABLE I. PERFORMANCE AND COMPARISON OF UWB TRANSMITTERS

Parameters	This work	[16]	[15]
Gaussian pulse derivative order	5th	5th	5th
Technology	0.18µm	0.18µm	0.50µm
Power supply	2V	1.8V	1.8V
PRR	100MHz	100MHz	20MHz
Pulse duration	300ps	420ps	2400ps
Pulse amplitude	90mVpp	51mVpp	160mVpp
Power consumption per pulse.	120µW	3.6mW	1.159mW
Circuit area (without pads)	23x46µm²	240x560µm²	--

6) Proposed Layout

Figure 9 shows the layout of the proposed UWB pulse generator circuit without the pads, where it is shown the areas of the input signal trigger, the triangle pulse generator, the delay circuit, the pulse shaping circuit, and the capacitor ***C***. Guard rings are used to minimize latch-up effects and interference between adjacent circuits. The complete pulse generator circuit occupies an area of 23x46µm², whereas the total array transmitter occupies only about 80x96µm². The capacitor occupies a large area of the chip (nominally 40%).

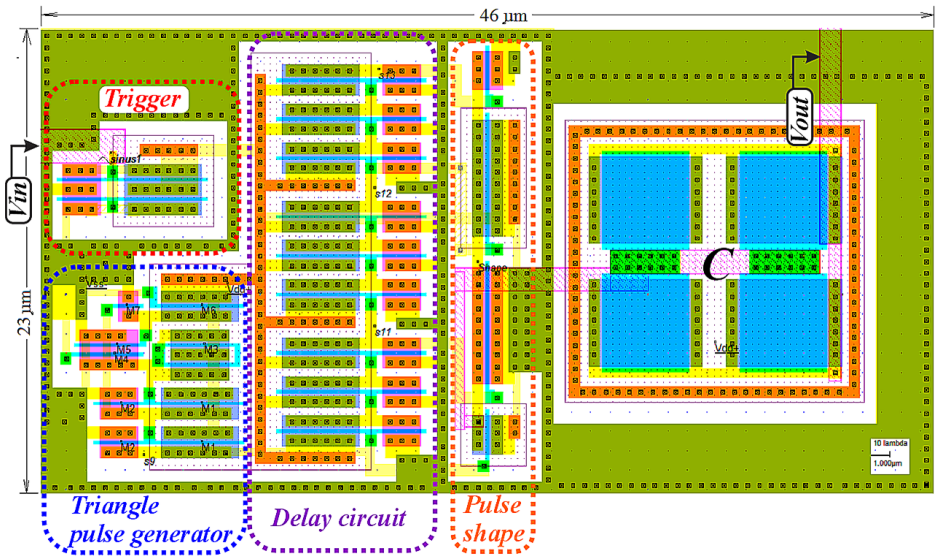

Fig 9. Layout of one pulse generator of the array UWB without pads.

B. Vivaldi antenna array

It is proposed an array of two antipodal Vivaldi antennas for the beamforming. The Vivaldi antennas belong to the class of aperiodic, continuously scaled, exponential curved antennas. The characteristics that make it suitable for UWB applications are that the Vivaldi antenna has theoretically constant beamwidth at unlimited operating frequency range [17, 18, 19]. This planar antenna is basically formed by a Microstrip Transition Line (MTL) and an exponential slot line radiator (ESLR). In the following, the MTL, ESLR and antenna array are presented.

1) Microstrip Trasition line

A MTL is defined as a transition line formed of a strip conductor and a ground plane isolated by a structural subtract (Fig. 10), usually with high dielectric constant (ε > 2), separating the ground plane of the microstrip line, both made by a thin metallic film, which is generally copper [14-21]. Since field lines are not totally contained in the substrate, the propagating mode in the strip line is not purely transverse electromagnetic (TEM), in this case is quasi-TEM [14-21].

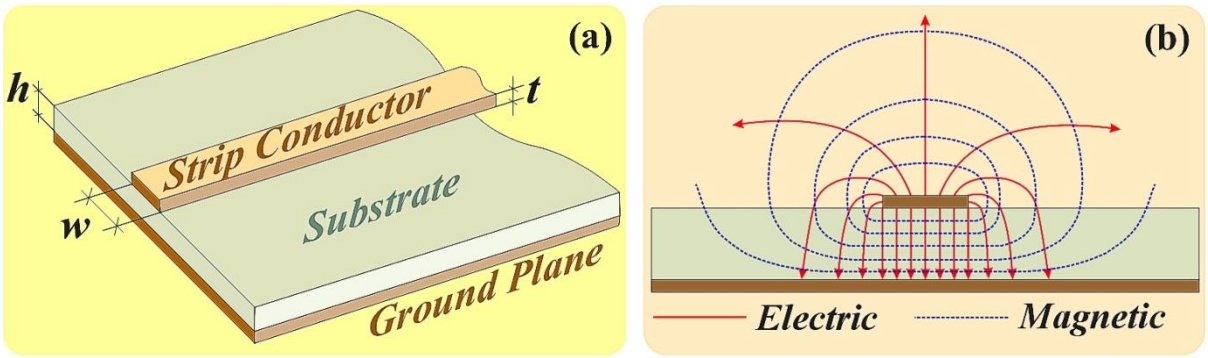

Fig. 10. Microstrip Transition line where h and t are the substrate and strip conductor thickness respectively, and w is the strip conductor width (a). A quasi-TEM analysis is represented (b) [20].

According to ref. [20], when the proportional relationship between ***w*** and h is greater than 1, the transition line has a characteristic impedance and an effective dielectric constant given by

$$Z_0 = \frac{120\ {}^{\pi}/_{\sqrt{\varepsilon_{eff}}}}{{}^{w}/_{h} + 1.393 + 0.667ln\left({}^{w}/_{h} + 1.444\right)} \tag{6}$$

where

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + 12\ {}^{h}/_{w}\right)^{-1/2} \tag{7}$$

In order to ensure a match with cables and circuits, that use a reference impedance of 50 Ω, the following parameters were used: the substrate chosen was the FR-4, whose dielectric constant is 4.3 and loss tangent of 0.025, the thickness (***h***) was chosen as 1 mm. It was used the analytical impedance calculation routine of the CST [8] to estimate the impedance of different widths (***w***). Therefore, the value of ***w*** = 1.815 with a $\boldsymbol{\varepsilon_{eff}}$ = 3.25 was obtained.

2) Exponential Slot Line Radiator

After obtaining the impedance matching between the circuit and the MTL, the goal is now to perform a smooth transition between the MTL and the signal propagation medium (air). For this transition, we considered a slot line radiator in the exponential tapered shape, since this ensures a relatively wide impedance bandwidth [17-19].

The opening function of the slot line radiator is shown in equations (8), (9) and (10), and is defined by the opening rate (***R***=0,105) and the points ***P1***(***x1,y1***) and ***P2***(***x2,y2***), as depicted in Fig. 11,

$$f(x) = c_1 e^{Rx} + c_2 \tag{8}$$

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where

$$c_1 = \frac{y_2 - y_1}{e^{Rx_2} - e^{Rx_1}} \tag{9}$$

And

$$c_2 = \frac{y_2 e^{Rx_2} - y_1 e^{Rx_1}}{e^{Rx_2} - e^{Rx_1}} \tag{10}$$

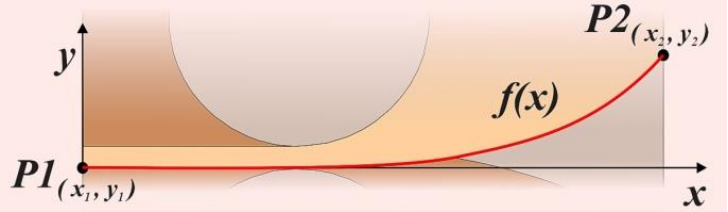

Fig. 11. Designed antipodal Vivaldi antenna, highlighting the Cartesian plane and the exponential shape of its opening.

3) Proposed Vivaldi antenna array

An array of two antipodal Vivaldi antennas for beamforming is proposed. The design parameters of dual-polarized array and Vivaldi antenna are shown in Fig. 12, and its respective dimensions in Table II.

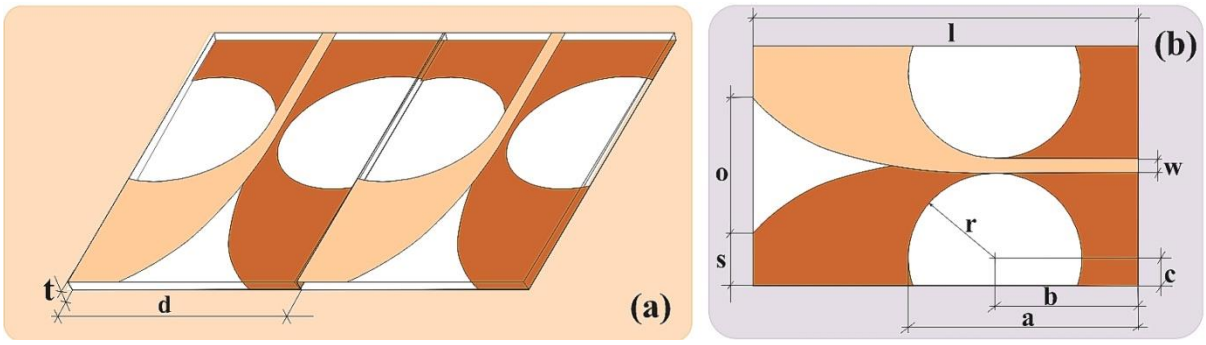

Fig. 12. (a) Key design parameters of array; (b) Key design parameters of the individual notch Vivaldi antenna.

TABLE II. DIMENSIONS OF THE ANTENNAS.

50Ω microstrip line	**w**		**b**			Units in mm.
	1,815		21,20			
Antenna dimensions	**l**	**o**	**s**	**r**	**c**	**a**
	58,40	22,66	7,89	13,40	1,90	34,60

Figure13 shows the simulated scattering parameter S11 of the antenna. It can be seen that after 6GHz the return loss is less than 10 dB.

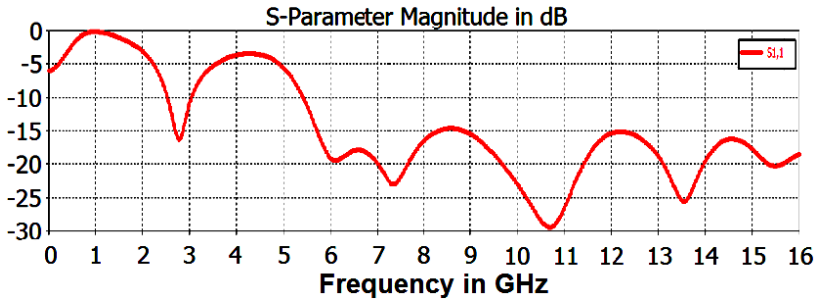

Fig. 13. Reflection Coefficient (S11) of proposed Vivaldi Antenna.

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III. SIMULATION RESULTS

The simulation of the complete Pulse Beamforming Transmitter in post-layout Spice model shows a pulse amplitude of 90mVpp and 300ps of pulse width, as well as a main lobe with gain of 5.5dB, (32º x 132º angular width). The beam can be steered between 20º and -17.5º relative to the θ angle Fig. 1(c), obtained through programmable delays ranging from 0 to 61ps, using the proposed PDC.

Table III and Fig. 14 show some possibilities for beamforming alongside with the required configuration parameters. Here, the first to second column are the PDC control words, in hexadecimal base; the third and fourth column contain the corresponding time delays; and, finally, fifth and sixth columns are of the beam radiated steering and gain results.

TABLE III. POSSIBLE CONTROL SETS AND RESULTS AT 7.5GHZ.

Programmable Delay Array		**Delay on the antenna input**		**Main Lobe**	
		1	**2**	**Simulated**	**Gain (dB)**
τ1	**τ2**	**Δτ(ps)**		**θ(º)**	
0Fh	00h	61	0	20	3.4
0Dh	00h	51	0	15	4.3
09h	00h	33	0	10	5.5
03h	00h	16	0	5	4.6
00h	00h	0	0	0	5.5
00h	03h	0	16	-5	4.3
00h	09h	0	33	-7.5	5.0
00h	0Dh	0	51	-15	3.4
00h	0Fh	0	61	-17.5	2.3

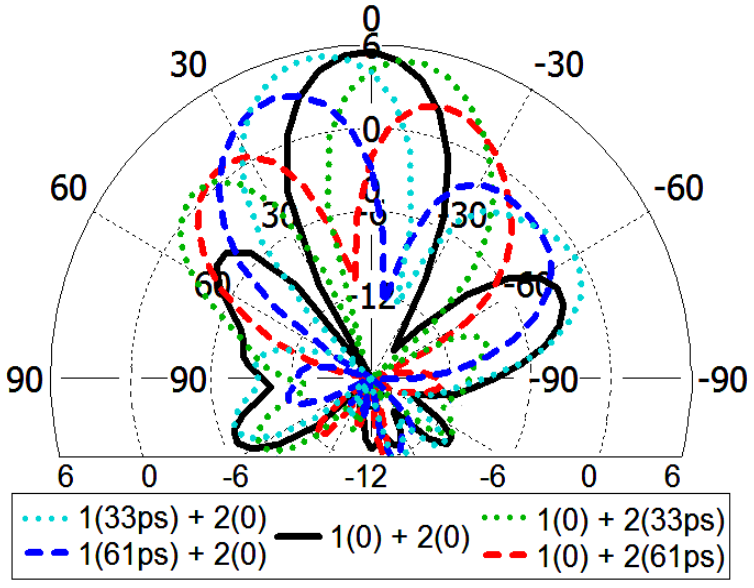

Fig. 14. Radiation pattern of the Fairfield (array) Gain (dB) x Theta (degrees) for some configuration parameters possibilities.

IV. CONCLUSION

In this paper the design of a new beamforming transmitter UWB pulse generator system composed

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of CMOS technology, as well as an antenna array design integrated with Spice and CST 2011 MW were presented. The simulation results showed a controllable beam steering between 20º and -17.5º for θ angle with an average gain of 5.5dB, 32º x 132º angular width. This control was achieved using a PDC array circuit that can generate delays digitally controlled from 0 to 61ps. The pulses obtained present 90mVpp amplitude and 300ps of pulse duration and a power consumption around 120μW per pulse using 2V power supply at PPR of 100MHz.

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