Materials Research. 2016; 19(5): 1201-1206
http://dx.doi.org/10.1590/1980-5373-MR-2015-0746

Poly(Vinyl Alcohol) Gate Dielectric Treated With Anionic Surfactant in C_{60} Fullerene-Based *n*-Channel Organic Field Effect Transistors

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Received: December 07, 2015; Revised: June 07, 2016; Accepted: August 20, 2016

We report on the preparation and performance enhancement of *n*-type low-voltage organic field effect transistors (FETs) based on cross-linked poly(vinyl alcohol) (cr-PVA) as gate dielectric and C_{60} fullerene as channel semiconductor. Transistors were prepared using bottom-gate top-contact geometry and exhibited field-effect mobility (μ_{FET}) of 0.18 $cm^2V^{-1}s^{-1}$. Treatment of the gate dielectric surface with an anionic surfactant, sodium dodecyl sulfate (SDS), passivates the positively charged defects present on the surface of cr-PVA, hence resulting in overall transistor performance improvement with an increase in μ_{FET} to 1.05 $cm^2V^{-1}s^{-1}$ and additional significant improvements in dielectric capacitance, transistor on/off current ratio and transconductance.

Keywords: *organic field-effect transistors, C_{60}, poly(vinyl alcohol), surfactant*

1. Introduction

Organic field effect transistors (FETs) have been a subject of much research over the past few decades due to the great technological up burst towards flexible organic electronics. However, *n*-type FETs were less investigated[1-3] than p-type ones, in part because of their unstable nature and high sensitivity to humidity and oxygen.[4,5] Nevertheless, owing to the importance of commercial applications involving organic complementary logic circuits, both *p*- and *n*-type FETs are in principle required.[6]

In the last years many results of high-mobility C_{60}-based field effect transistors have been reported exploiting single crystals, ensuing expensive techniques and methods,[3,7-9] or either preparing devices that are eventually not compatible with flexible substrates.[10,11] In this context, in addition to enhanced performance, cost-effectiveness, simplicity of device preparation and compatibility with flexible substrates is highly desired.

The use of cross-linked poly(vinyl alcohol) (cr-PVA) as gate dielectric in transistors is a topic showing intense research activity[12-16] and there are strong evidences that the surface of cr-PVA consists of negatively and positively charged defects that act as charge traps or scattering centers and hinder charge flow near the insulator/semiconductor (I/S) interface. Transport hindrance is to a great extent imposed by the topology of the equipotential electrostatic surface near the I/S interface instead of being simply due to the surface morphology. In this context, passivation/neutralization of such traps is necessary to ameliorate device performance. Treatments have recently successfully solved this problem in devices based on *p*-type channel semiconductors, poly(3-hexylthiophene-2,5-diyl)[17-19] and copper phthalocyanine.[20,21] As transistor size gets smaller, many undesirable effects come into play and nanometrically small defects and traps play a significant role, impairing device performance.

In a grounded-source FET, the gate voltage V_{GS} aims the accumulation of mobile charges at the vicinity of the I/S interface, while the drain voltage V_{DS} is applied to promote the charge transport along the channel. Due to the simultaneous application of both voltages, the thickness of the effective channel (region of the channel effectively participating in the charge transport process) varies along the channel. It shows a minimum, denoted channel bottleneck, near to the source terminal. Thus, since this bottleneck is adjacent to the I/S interface, the performance of the FET is limited due to the hindering of charge transport by the cr-PVA surface traps, which is evidenced if charge-carrier field-effect mobility (μ_{FET}) is plotted as a function of channel bottleneck thickness (l_0).[20]

In this work we report on the preparation of transistors with a solution-processed flexible substrate compatible organic gate dielectric, cr-PVA and C_{60} channel semiconductor. In addition, we show an easy and cost-effective method to suppress the action of negative charge traps present on the surface of cr-PVA using the deposition of an anionic surfactant, sodium dodecyl sulfate (SDS), in turn obtaining an enhanced transistor performance. To get a better insight regarding the charge transport we support our discussion by showing the variation in μ_{FET} with respect to l_0, which provides important information regarding the variation of μ_{FET} as a function of distance from the I/S interface.

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2. Experimental Procedure

Device fabrication and characterization procedures are reported in detail in Ref.[21] Briefly, Al gate was evaporated onto glass substrate and PVA was thermally and UV treated to obtain cross-linked PVA (cr-PVA) after which Al layer was covered by spin-coating cr-PVA on top of it. SDS (supplied by Sigma-Aldrich, ACS Reagent > 99%) was dissolved in water at a concentration of 3.0 mg/mL and stirred for one hour at 60°C. A ~20 nm SDS layer was then spin-coated on the Al/cr-PVA films at 1500 rpm for 60 s and sequentially annealed in vacuum for 30 min at 100°C followed by C_{60}(Sigma-Aldrich, 99.5%) layer deposition. C_{60} was thermally evaporated using shadow mask to control the layer geometry. Shadow mask patterned gold was then evaporated to obtain source and drain terminals. Devices were then encapsulated using 4.5 mg of PIB (polyisobutene, molecular mass: 850-900 g/mol, density: 0.88 mg/mm^3, viscosity: 2.5×10^5 SUS at 21°C, supplied by Polibutenos S.A Indútrias Químicas) that was dropped onto the device area and covered with a 0.1 mm thick glass slice, as detailed reported by Toniolo et al.[22] Transistor structure and chemical structure of C_{60} are shown in Figure 1.

Capacitance measurements were performed in Al/cr-PVA/Au and Al/cr-PVA/SDS/Au sandwich structures using an Agilent 4284-A LCR meter, at a frequency of 1 kHz. Transistor characterization was carried out using a Keithley 2602 dual source meter in air in the dark.

3. Results and Discussions

Charge transport in OFETs is governed by several mechanisms, including the amount of charge accumulated at the I/S interface following appliance of a potential between gate and channel semiconductor. Once drain-source voltage (V_{DS}) is applied, an electric field along the *x*-direction results in the transport of charge along the channel from source to drain (Figure 2). The drain-source current (I_{DS}) is expressed in saturation regime ($V_{DS}>V_T$) as:

$$I_{DS} = \frac{W\mu_{FET}C_i(V_{GS}-V_T)^2}{2L} \quad (1)$$

where W is the channel width, μ is the field-effect charge carrier mobility, V_{GS} is the applied gate voltage, V_T is the threshold voltage and L is the channel length. Increasing V_{GS} restricts I_{DS} very close to the I/S interface, essentially reducing the effective channel thickness, and hence the very first few molecular layers of the interface determine the charge transport properties. The drift-diffusion equation allows estimating the minimum effective channel thickness (l_0) perpendicular to the I/S interface, along the *z*-direction,[23] in the effective channel bottleneck. It can be expressed as:

$$l_0 = \frac{4\varepsilon kT}{eC_i(V_{GS}-V_T)} \quad (2)$$

where ε is the channel semiconductor dielectric constant, k is the Boltzmann constant, T is the absolute temperature, e is the electronic charge and C_i is the gate dielectric specific capacitance.

Figure 3a shows the I_{DS} versus V_{DS} plots for the gate voltage V_{GS} varying between 0 and 5 V measured in samples with and without SDS-treated cr-PVA, for comparison. Similar to the behavior observed in conventional FETs with increasing V_{DS}, the I_{DS} initially increases linearly, then levels off gradually, and approaches a saturated value. The I_{DS} value is improved when cr-PVA layer is treated with SDS. One important aspect to be kept in mind while working with C_{60} semiconductor is that, in general the *n*-type behavior of organic semiconductor is reasonably sensitive to physically and chemically adsorbed O_2 and/or H_2O molecules, which can possibly generate electron traps, hence suppressing the charge transport.[24-27] In order to protect the device from the adsorption of O_2 or H_2O molecules, the C_{60} layer was encapsulated using PIB as described above.

The effective channel thickness bottleneck limits the charge transport because of the presence of charge traps or dipoles at the I/S interface owing to the surface of the gate dielectric.[28] This is then reflected in the form of low μ_{FET} and hence low I_{DS} as seen in the output characteristics, $I_{DS}(V_{DS})$ (Figure 3a). The surface of cr-PVA consists of charge traps and dipoles acting as charge trapping or scattering sites.[15,16] Our results indicate that the passivation of negatively charged

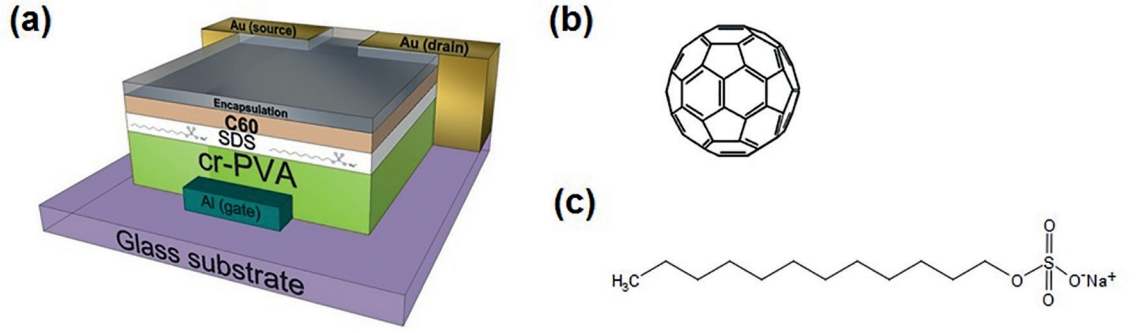

Figure 1: (a) Schematic structure of the SDS-treated OFET, (b) chemical structure of C_{60}, and; (c) chemical structure of SDS.

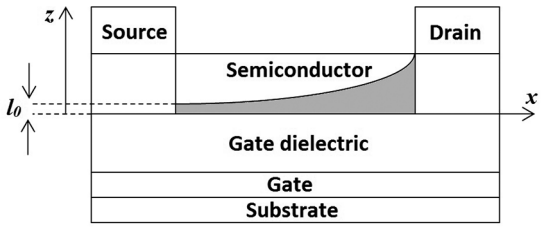

Figure 2: Schematic representation of FET showing the variation of effective channel thickness *l* along the *x*-direction, with the effective channel represented in gray.

centers on the cr-PVA surface results in enhancement of charge accumulation at the I/S interface, resulting in an increase in C_i, μ_{FET}, I_{DS} (Figure 3a) and transconductance, $g_m \equiv dI_{DS}/dV_{GS}$ (Figure 3d). This seems to be contradictory to the observed displacement of V_T to a more positive value (Table 1). But as can be observed in Figure 3c, the slope of the curve depends on the V_{GS} range, as a consequence implying in a large uncertainty in the V_T value. For this same reason, the use of the transfer characteristics, $I_{DS}(V_{GS})$ (Figure 3b) and linear best-fit plot for mobility (Figure 3c) also depends on the V_{GS} interval, despite indicating a clear trend to higher mobility. It can clearly be seen that the deposition of SDS on top of the cr-PVA layer results in significant device parameters enhancement. SDS is assumed to be working as a part of the dielectric layer, as an extension of the gate dielectric, since when compared to the untreated devices, no increase in the OFF current of the SDS-treated ones is observed. Device parameters of both untreated and SDS-treated transistors are summarized in Table 1.

The Dependence of μ_{FET} on V_{GS} and on l_0 can be determined in saturation regime ($V_{DS} > V_T$) (Figure 4) using[29]

$$\mu_{FET} = \frac{2L}{WC_i}\left[d\left(I_{DS}\right)^{1/2}/dV_{GS}\right]^2 \qquad (3)$$

which gives direct information about the variation of mobility with respect to the different bottleneck thicknesses induced by V_{GS}. One important feature observed in the μ_{FET} *vs.* l_0 plot (Figure 4b) is that, apart from the magnitude of I_{DS} being higher, the shape of the curve is different. It can be seen in Figure 4a that μ_{FET} initially increases with increasing V_{GS}, however, at V_{GS}-$V_T \approx 2.3$ V (untreated transistor) and V_{GS}-$V_T \approx 1.15$ V (SDS-treated transistor), a decreasing μ_{FET} trend is observed, which can be attributed to the presence of charged defects present on the surface of cr-PVA. These charged defects in principle act as static charges forming energy valleys (negatively charged defects) and hills (positively charged defects) near to the I/S interface, since higher V_{GS}-V_T

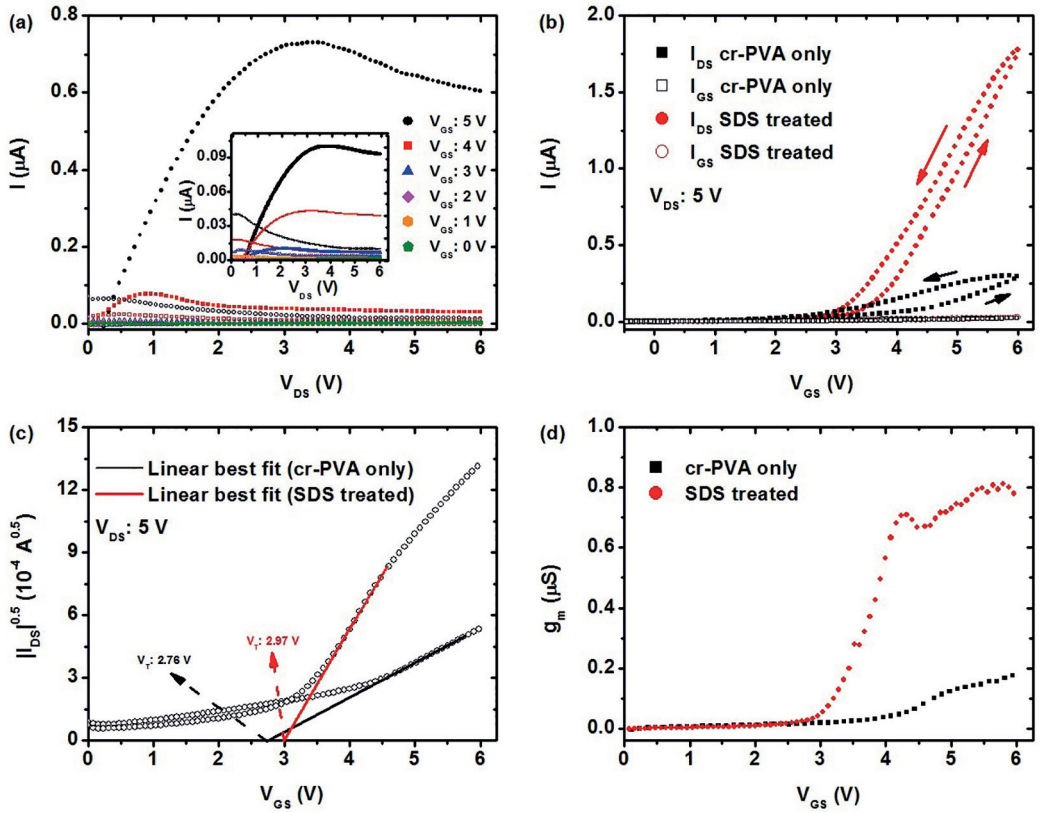

Figure 3: (a) Output characteristics ($I_{DS}(V_{DS})$) of SDS treated device (inset shows $I_{DS}(V_{DS})$ of untreated device) (open circles correspond to $I_{GS}(V_{DS})$); (b) transfer characteristics ($I_{DS}(V_{GS})$); (c) linear best-fit plots for mobility and V_T calculation (the curves are taken in the increasing V_{GS} regime), and; (d) transconductance (g_m) as a function of V_{GS}, for untreated and SDS treated devices.

Table 1: Device performance parameters for untreated and SDS treated C_{60}-based *n*-type FETs. The g_m and g_m/W values were calculated at V_{DS} = 6 V.

Device	V_T	μ (cm^2 V^{-1} s^{-1})	C_i (nF cm^{-2})	I_{on}/I_{off}	g_m (μS)	g_m/W (S cm^{-1})
cr-PVA only	2.76±0.30	0.18±0.15	15.18	70	0.17	8.50×10^{-7}
SDS treated	2.96±0.10	1.05±0.08	25.38	565	0.81	4.05×10^{-6}

values correspond to lower l_0 (Figure 4b). At lower V_{GS}, the flow of charges is distributed more equally in the channel layer, to a great extent far from the I/S interface. Hence, there is limited interaction of charge carriers with the I/S interface charged defects, whereas, with increasing V_{GS}, the flow of charge carriers occurs very near to the interface in the channel bottleneck, being hindered by these charge defects originated electrostatic potential variations. The transistor in which the cr-PVA layer is treated with SDS exhibits flow of charge carriers at higher mobility values throughout the bottleneck (Figure 4b), which is attributed to a lower density of charged defects at I/S interface and the highest μ_{FET} value (1.05 cm^2 V^{-1} s^{-1}) is observed at around l_0 = 9 nm.

Sworakowski and co-workers used a mobility dependence on the distance z to the interface given by the function $\mu \propto [1 - \exp(-z/\lambda)]$ (where λ is a constant of the order of the molecular dimensions) to account for the interface neighborhood imposed mobility decay.[30,31] The variation in the average mobility with respect to l_0, when the effective channel bottleneck reaches its minimum thickness ($|V_{GS}-V_T| \rightarrow \infty$) can then be described using:

$$\overline{\mu}_{FET} = l_0^{-1} \int_0^{l_0} \mu(z)\,dz = \mu_0 l_0^{-1} \int_0^{l_0} [1 - \exp(-\tfrac{z}{\lambda})]\,dz = \mu_0\{1 - \tfrac{\lambda}{l_0}[1 - \exp(-\tfrac{l_0}{\lambda})]\} \quad (4)$$

where μ_0 is the bulk mobility. It is important to keep in mind the limitations of this model, since around 30 nm, the effective channel thickness reaches full thickness of the C_{60} layer near to the drain electrode (at low V_{GS}), hence the further decrease in mobility for larger l_0 is witnessed.

Previous reports on C_{60}-based OFETs have usually stressed on enhancing device performance by improving the metal contact/channel interface by reducing the contact resistance using several techniques.[32,33] Quite recently Du et al. demonstrated that μ_{FET} of C_{60}-based transistors can be improved by modifying the I/S interface properties. In their work they achieved a highest μ_{FET} of 0.31 cm^2 V^{-1}s^{-1}.[34] In top-contact FETs, there are typically two forms of resistances: metal contact/channel interface resistance and the organic channel resistance itself. Contact resistance can be reduced by tuning the injection barrier, whereas, for C_{60}-based OFETs very few studies are found dealing with the reduction of the channel resistance through the improvement of the transport in the vicinity of the I/S interface. Our work was aimed to minimize the effect of charged defects present on I/S interface and to enhance the properties of this region to obtain an overall enhanced OFET performance. After SDS treatment a better charge transport in the channel close to the I/S interface is observed, hence resulting in a *ca.* 5-fold increase in μ_{FET} and g_m and additionally, a *ca.* 8-fold increase in I_{on}/I_{off}.

4. Conclusions

In summary, this work was concerned with the development of C_{60}-fullerene based *n*-channel OFETs with cr-PVA gate dielectric. The performance of these devices

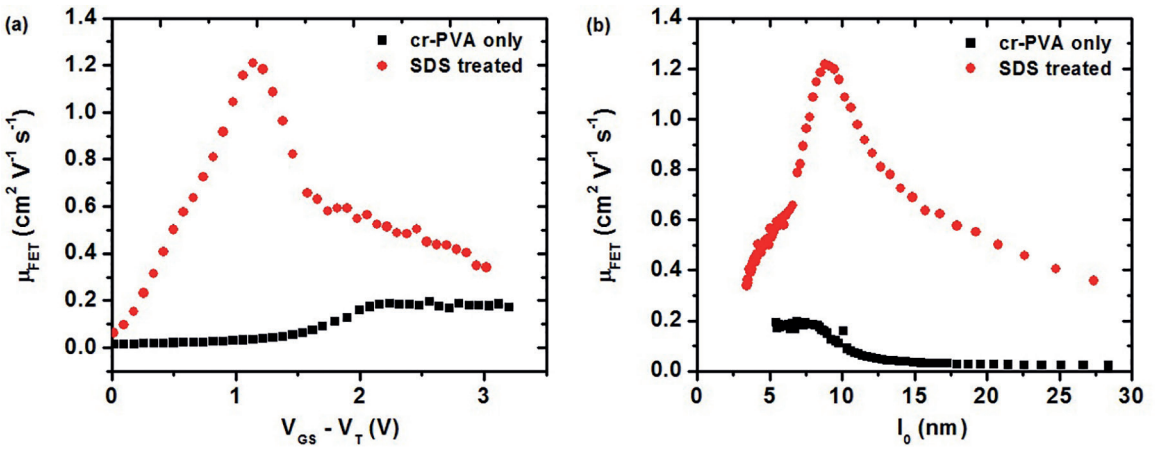

Figure 4: Field effect charge carrier mobility as a function of: (a) V_{GS}-V_T, (b) minimum effective channel bottleneck thickness (l_0), for untreated and SDS treated transistors. In both cases V_{DS} = 5 V.

was not found to be up to the mark when compared with previous reports on C_{60}-based OFETs. Hence in the quest of improving overall performance, a cost-effective but efficient method was applied, involving deposition of an additional layer of sodium dodecyl sulfate (SDS) anionic surfactant on top of the gate dielectric. The SDS acted as a treating agent, passivating the positively charged defects present on the surface of cr-PVA. Field-effect mobility μ_{FET} was analyzed as a function of channel bottleneck thickness and an increase in μ_{FET} was observed after SDS treatment. SDS acted as a part of cr-PVA, significantly improving the specific capacitance and crucial parameters including μ_{FET}, g_m and on/off current ratio.

5. Acknowledgements

The authors would like to thank CNPq and CAPES for research grants and fellowships.

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