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Design and Characterization of Au/CdSe/GeO_2/C MOSFET Devices

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Herein, metal-oxide-semiconductor fields effect transistors (MOSFET) are fabricated and characterized. p−type germanium dioxide coated onto Au/n-CdSe substrates and top contacted with carbon point contacts is used to form the MOSFET devices. The structural investigations which were carried out with the help of X-ray diffraction technique revealed large lattice mismatched polycrystalline layers of CdSe and GeO_2. The design of the energy band diagram has shown the formation of two Schottky arms (Au/n−CdSe, C/GeO_2) at the interfaces of the n−CdSe/p−GeO_2 layers. The capacitance-voltage characteristics which are recorded in the frequency domain of 1.0-50.0 MHz revealed the ability of formation of NMOS and PMOS layers. The signal frequency controlled built in potential is tunable in the range of 2.34 and 5.18 eV. In addition, the conductance and capacitance spectral analyses in the frequency domain of 10-1800 MHz revealed the domination of current conduction by tunneling and correlated barriers hoping below and above 760 MHz, respectively. In addition to its features as MOSFET devices, the Au/CdSe/GeO_2/C hybrid devices are found to be appropriate for use as microwave cavities.

Keywords: *CdSe/GeO_2, MOSFET, band diagram, microwave cavity.*

1. Introduction

Germanium dioxide thin films have occupied the interest of researchers since years. It is regarded as promising material which can be employed in more than one technology sector. As for examples, GeO_2 is used in lithium batteries owing to their capability of charge storage[1]. Porous GeO_2(s)/Ge(c) nanostructures which were used as lithium-ion battery anode revealed capacity of 1.33 Ah/g at a current density of 0.1 A/g[1]. Germanium dioxide crystals are also regarded as smart materials for the production of piezoelectricity. Temperature dependent studies on this crystal indicated the ability to retain large piezoelectric properties in the temperature range of 20-600 ^{o}C[2]. In addition, because of the ultra-wide band gap of GeO_2 and high electron and hole mobility values it is nominated for future power electronics[3]. The electron and hole mobility's of the germanium oxide reached 377 and 29 cm^2/Vs, respectively. Moreover, deposition of ultrathin GeO_2 layers onto $MoTe_2$/Ge heterojunctions successfully reduced the dark current density of the $MoTe_2$/GeO_2/Ge photodetectors from 0.44 μA/μm^2 to 0.03 nA/μm^2[4]. As a result, the photosensitivity is enhanced and the responsivity increased to 15.6 A/W. Furthermore, Germanium oxide nanoparticles which were prepared from the bulk GeO_2 powders using the hydrothermal technique are mentioned exhibiting characteristics of electrically erasable memory devices[5].

Because of the above mentioned smart features of germanium dioxide, here in this work, we are motivated to find another type of applications for the GeO_2 thin films. For this reason, germanium dioxide thin films are coated onto Au/CdSe substrates and top contacted with carbon point contacts to form hybrid device structure. The Au/CdSe substrates are selected because they reveal Schottky barriers and able to behave as band stop filters in the microwave range of frequency[6]. The constructed Au/CdSe/GeO_2/C hybrid devices which are formed of two Schottky arms connected *pn* junctions are structurally and electrically investigated. The capacitance-voltage characteristics in the frequency domain of 1.0-50 MHz are recorded and analyzed. In addition, the capacitance and conductance spectra in the frequency domain of 10-1800 MHz are considered in detail.

2. Experimental Details

Gold substrates were coated onto ultrasonically cleaned glasses prior for the fabrication of CdSe base layers. The Cadmium selenide thin films were evaporated onto Au substrates using NORM VCM-600 vacuum evaporator at vacuum pressure of 10^{-5} mbar. The source material was CdSe crystal lumps (99.995% Alpha Aesar). Using a high purity GeO_2 powders (Alpha Aesar 99.99%), GeO_2 films of thicknesses of 500 nm were then deposited onto the Au/CdSe films. The films thicknesses were measured with the help of Inficon STM-2 thickness monitor. The structure of the films was investigated with the help of MiniFlex 600 X-ray diffraction unit. The X-ray diffraction patterns were recorded as scanning speed of 0.5^{o} / min. The produced Au/CdSe/GeO_2 films were masked to locate circular carbon

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point contacts. The conductivity type of the CdSe and GeO_2 was determined by the hot probe technique. The capacitance-voltage characteristic, capacitance spectra and conductance spectra were measured with the help of Agilent 4291B 1.0 M–1.8 GHz impedance analyzer.

3. Results and Discussion

The metal-oxide-semiconductor fields effect transistors (MOSFET) which are illustrated in the inset of Figure 1 are fabricated by depositing $n-$CdSe onto Au substrates and coating $p-$$GeO_2$ onto the Au/$n-$CdSe layers. The resulting Au/$n-$CdSe/$p-$$GeO_2$ interfaces are painted with carbon point contacts of areas of $7.85\times10^{-3}\ cm^2$. The X-ray diffraction patterns for the produced MOSFET devices before the painting of carbon point contacts are shown in Figure 1. The observed diffraction peaks indicate the polycrystalline structure for the deposited layers. The diffraction peaks are indexed in accordance with the existing (Powder Diffraction File) PDF cards for Au (PDF Card No: 00-001-1172), CdSe (PDF Card No:00-002-0330) and GeO_2 (PDF Card No: 85-1515) The lattice parameters for the cubic Au, hexagonal CdSe and hexagonal GeO_2 are $a=b=c=4.08\,Å$, $a=b=4.300$ Å and $c=7.020$ Å and $a=b=4.987$ Å and $c=5.652$ Å, respectively. Our exact calculations using Crystdiff software packages reveal respective lattice parameters of $a=b=c=4.046\,Å$, $a=b=4.423$ Å and $c=6.914$ Å and $a=b=4.918$ Å and $c=5.625$ Å. The lattice mismatches percentages ($\Delta_a\%=100(a_{CdSe}-a_{Au})/a_{CdSe}$)[7] between the cubic Au and hexagonal CdSe cells along the a and $c-$axes are $\Delta_a=8.52\%$, $\Delta_c=41.48\%$. The lattice mismatches between CdSe and GeO_2 are 10.06% and 22.92% along the $a-$ and $c-$axes respectively. Large lattice mismatches causes interfacial stresses and forms three dimensional quantum confinement[8,9].

From electrical point of view, the work function ($q\phi_{Au}$) of Au is 5.34 eV[6]. It is larger than the work function of $n-$CdSe (4.80 eV). The difference between the two work function forms a Schottky contact between at the Au/n-CdSe interfaces. The work function of $p-$$GeO_2$ is not well defined. The electron affinity of GeO_2 is 2.24 eV and the energy band gap is 5. 35 eV[10] are known. Hence the work function of GeO2 can be calculated. Particularly, extrapolation of the published conductivity –reciprocal temperature variations for the Ag/GeO_2/Ag reveals conductivity activation energy of $E_\sigma=17.4$ meV above the top of the valance band. This means that the Fermi level is located at $E_F=E_\sigma/2=8.7$ meV. The value of the work function of GeO_2 is then 7.58 eV. The work function of $p-$$GeO_2$ is much larger than that of carbon (5.10 eV) leading to the formation of another Schottky arm at the C/GeO_2 side. The interface between $n-$CdSe and $p-$$GeO_2$ establishes a pn junction device. The overall established MOSFET device is formed from two Schottky arms attached by a pn junction. The energy band diagram for the device is shown in Figure 2. Three different built in potential of values of $qV_{bi-1}=\left|q\phi_{Au}-q\phi_{CdSe}\right|=0.54$ eV, $qV_{bi-2}=\left|q\phi_{GeO_2}-q\phi_{CdSe}\right|=2.78$ eV and $qV_{bi-3}=\left|q\phi_C-q\phi_{GeO2}\right|=2.48$ eV at the Au/CdSe, CdSe/GeO_2 and at C/GeO_2 interfaces need to be overcome to operate the device properly.

As practical verification of the proposed energy band diagram, the capacitance-voltage characteristics are recorded in the frequency domain of 1.0-50.0 MHz. Illustrative examples of the measured $C-V$ characteristics are shown in Figure 3a, b and c. The $C-V$ characteristics display typical MOSFET characteristics. It seems that the device is composed of two MOS devices. Namely, the device displays an inversion mode of PMOS transistor when reverse biased and an inverted mode of operation of NMOS characteristics when forward biased[11]. At the PMOS arm, when activated by lowering the voltage below ~ 0.40 V, the device allows the conduction of holes reaching a minimum capacitance value at $V=-0.11V$. While on the other hand, when the NMOS is operated an inversion layer in the GeO_2 (p- layer) is created forming $n-$channel. Conduction in this channel is dominated by electrons. For this channel, the larger the signal frequency, the larger the applied voltage needed to reach the strong inversion condition. It is also noticeable that the change in the capacitance values as the devices switches from strong inversion to weak accumulation states (illustrated in Figure 3a) become less pronounced as the signal frequency increases. As for examples, when the device is in the PMOS mode, the capacitance decreases from 625 pF to 600 pF, from 252 pF to 242 pF and from 172 pf to 171 pf as the signal frequency increases from 5.0 MHz to 10 MHz and reaches 50 MHz, respectively. This behavior is assigned to the charge dynamics. Namely, charges in the depletion layer of PMOS capacitors increase as $\sim\sqrt{\phi}$ (ϕ: surface barrier height)

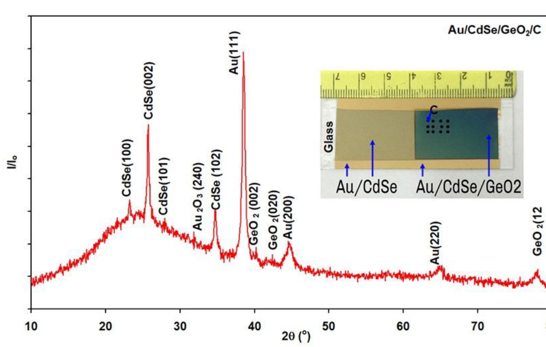

Figure 1. The X-ray diffraction patterns for Au/CdSe/GeO_2 films. Inset-1 shows the geometrical design of the MOSFET devices.

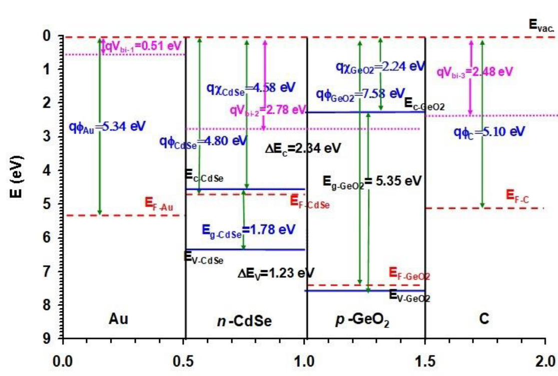

Figure 2. The energy band diagram for the MOSFET Au/CdSe/GeO_2/C devices. The pink colored dashed lines show the lowering of the vacuum level.

so depletion capacitance decreases as the inverse. Slowly varying signals gives the sufficient time for minority carriers to be generated, drift across depleting regions, or recombine. In contrast to this fact, when signal frequency is high inversion layer carriers can't respond and do not contribute[7]. Analyses of the recorded capacitance-voltage characteristics in accordance with the well know equation, $C^{-2} = 2\left(V - V_{bi} - \frac{kT}{q}\right) / (qA^2 \in_s N)$, for capacitance in depletion region allow determining the MOSFET device parameters. Namely, for NMOS and PMOS modes which are effective in the frequency domain of 1.0-5.0 MHz, the fitting of the equation demonstrated in Figure 3d reveal straight lines. From these slopes and intercepts, it was possible to determine the free charge carrier density (N), the built in potential (qV_{bi}) and the depletion width (W). Substituting the value of the high frequency dielectric constant ($\in_s$) as 3.88 (experimentally determined), qV_{bi}, N and W values were determined. The signal frequency effects on the built in potential, on the free charge carrier density and on the depletion width are readable from Fig .4 (a), (b) and (c), respectively. It is clear from the figure that the built in voltage initially decreases with increasing signal frequency for both of the PMOS and NMOS arms. As for examples, for NMOS channel starting from a value of 5.18 eV recorded at signal frequency of 1.0 MHz, V_{bi} decreases reaching a minima of 2.34 eV at 3.0 MHz. For larger frequency values, the built in potential, increases with increasing signal frequency exhibiting a value of 3.46 eV at signal frequency value of 5.0 MHz. Similar trend of variation is also observable when the device operates in the PMOS mode. Namely, the built in potential decreases from 4.54 eV at 1.0 MHz to 2.36 eV at 3.0 MHz and reaches 3.46 eV at 5.0 MHz. In accordance with the presented energy band diagram, values of built in potential close to 5.18 eV should be related to depletion through the CdSe/GeO_2 with $qV_{bi-2} = 2.78 eV$ and the Schottky shoulders C/GeO_2 whose unbiased built in potential is $qV_{bi-3} = 2.48 eV$. The sum of these two potential reveals built in potential of ($qV_{bi-23} = qV_{bi-3} + qV_{bi-2}$) of 5.26 eV. Since setting the PMOS channel on switches the NMOS off, then the second Schottky arm (Au/CdSe) is at reverse bias and its potential is subtracted leading to a net potential of $qV_{bi} = qV_{bi-3} + qV_{bi-2} - qV_{bi-1}$ =4.78 eV which is close to the experimentally determined as 4.54 eV for PMOS channels at 1.0 MHz[7]. On the other hand, while the free charge carrier density continuously decreases, the depletion width increases with increasing signal frequency. The values of N follow a power law defined by the function $N = Const.F^s$ with s being ~1.99 and 1.80 for PMOS and NMOS channels, respectively. As also appears in Figure 4c, the depletion width increases with increasing signal frequency. The decrease in the free carrier density with increasing signal frequency is ascribed to the inability of the free charge carriers to orient with oscillatory incident electric signals[11].

It is worth noting that calculations that targeted estimation of the V_{bi}, N and W at higher frequency values ($F > 5.0$MHz) revealed built in potential values larger than 10 eV. It indicates the invalidity of the depletion approximation method in the high frequency region. The capacitance response to biasing voltage at high frequencies arises from the diffusion capacitance which usually appears under forward biasing conditions for *pn* junction devices. However, as our constructed device is hybrid structure formed of two Schottky arms connected to *pn* junctions, forward biasing of one of the Schottky arms will necessary reverse the biasing of the other. For this reason, the diffusion capacitance appears for both of the NMOS and PMOS devices[7].

In an attempt to explore the role of growth rates and thickness on the performance of the MOSFET devices, we have re-prepared the devices by coating GeO_2 layer of thickness of 250 nm at high and slow deposition rates of 11.7 $Å/s$ and 5.2 $Å/s$, respectively. The measured $C-V$ characteristics are shown in Figure 5a and b, respectively. It is clear from the figure, that the slower the deposition rate,

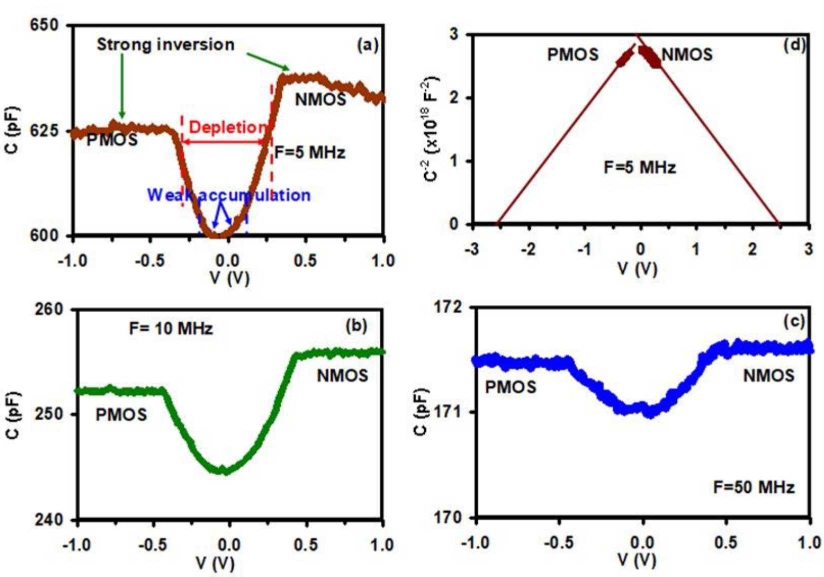

Figure 3. the capacitance-voltage characteristics for the Au/CdSe/GeO_2/C MOSFET devices recorded signal frequency of (a) 5.0 MHz, (b) 10 MHz and (c) 50 MHz. (d) the $C^{-2}-V$ variations for the MOSFET devices recorded at signal frequency of 5.0 MHz.

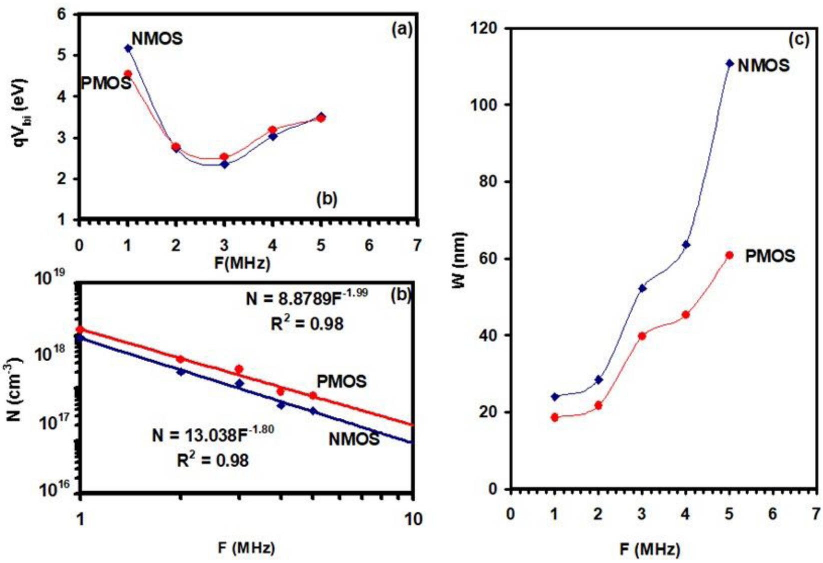

Figure 4. (a) the frequency dependent (a) built in potential, (b) free carrier density and (c) depletion width of the imaginary part of the dielectric spectra and (c) the photocurrent-illumination intensity dependence of the Au/CdSe/GeO_2/C MOSFET devices.

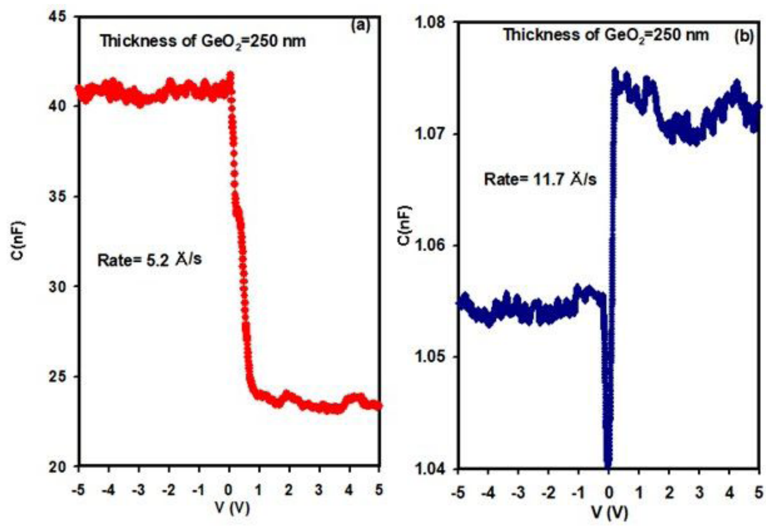

Figure 5. The capacitance-voltage characteristics for Au/CdSe/GeO_2/C devices with GeO2 layer thickness of 250 nm prepared at (a) slow and (b) high deposition rates.

the more accurate the collected data and the more stable the capacitance response to voltage excitations. Compared to the 500 nm thick GeO_2 films which were prepared at slow deposition rates (Figure 3a), the $C-V$ curve of the 250 nm thick device indicates the formation of PMOS device and the inverted NMOS channel is absent. In addition, the value of the capacitance at particular voltage is much larger for the CdSe coated with 250 nm GeO_2 layers at slower rates. The effect of thickness and deposition rate is also evident from the calculated free carrier density. The free carrier density for films prepared at slow rates decreased from $2.18\times10^{20}cm^{-3}$ to $7.24\times10^{17}cm^{-3}$ as the film thickness is increased from 250 to 500 nm. The large number of free carriers ($\sim10^{20}$ cm^{-3}) indicates the existence of short scattering times and low mobility of charge carriers. While on the other hand, increasing the thickness is mentioned enhancing the mobility of charge carriers in thin film transistors. This is just because the thickness of the active channel layer is increased[12]. Similar conditions apply for the films prepared at faster rates. For GeO_2 layers of thicknesses of 250 nm prepared at fast rates the free carrier density is 2.4×10^{18} cm^{-3}. It is mentioned that high deposition rates causes poor crystallinity. In this case, some oxygen atoms might not be bonded leading to the high number of free charge carriers[13].

Figure 6a illustrates the capacitance spectra for the Au/CdSe/GeO_2/C MOSFET devices being recorded at low biasing voltage (V=0.10 V) and in a wide range of frequency (10-1800 MHz). As seen from the figure, the capacitance sharply decreases with increasing signal frequency. The larger the frequency, the more pronounced

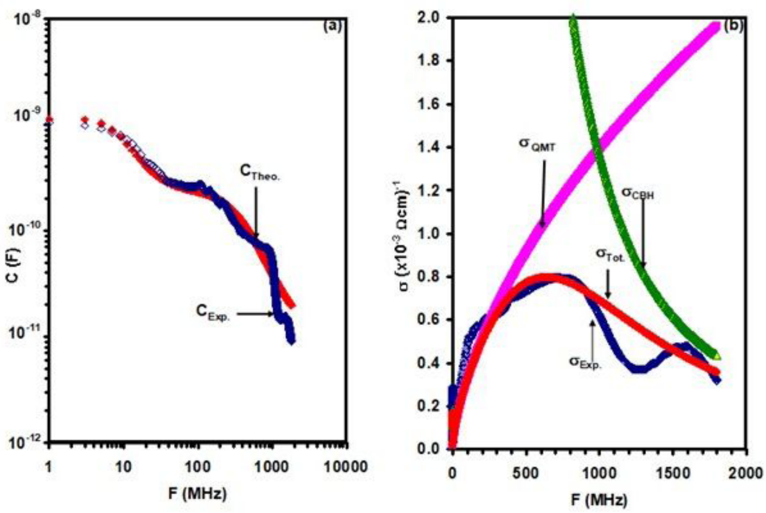

Figure 6. (a) The capacitance and (b) the conductance spectra for the Au/CdSe/GeO_2/C MOSFET devices recorded in the frequency domain of 10-1800 MHz. The red colored circles in the figures show the fitting of equation 1 and equation 2.

the decrease. To explain the origin of the capacitance spectra we employ the previously reported Qasrawi-Ershov method. In that approach, the capacitance is assumed to be composed of geometrical and dynamical parts known as C_o and C_1, respectively. The dynamical part of the capacitance is due to holes and due to electrons oscillatory motion. The total capacitance take the form[14],

$$C(w) = C_o + \frac{a_n \tau_n}{1+(w-w_n)^2 \tau_n^2} - \frac{a_p \tau_p}{1+(w-w_p)^2 \tau_p^2} \quad (1)$$

In the above equation, a_n and a_p are parameters in the units of F/s and accounts for electrons and holes time dependent capacitances, respectively. τ_n and τ_p are the respective scattering times and w_n and w_p are the plasmon frequency values arising from electron-plasmon interaction at the surface of CdSe and from the hole-plasmon interaction at the GeO_2 side. The fitting of Equation 1 is shown by red colored circles in Figure 6a. The fitting allowed determining the tabulated physical parameters for the MOSFET devices under study. The tabulated data suggests that the rate of change of the capacitance with time (a_n, a_p) is positive for electrons and negative for holes. The total capacitance are positive indicating that the diffusion capacitance (above 5.0 MHz) is dominated by the minority carriers (electrons). The relaxation (scattering) times for electrons being 18.0 nm is ~43 times larger than that of holes ($\tau_p = 0.42$ ns). The plasmon frequency for both dynamical capacitances is the same. In comparison with the previously reported data about CdS/Sb_2Te_3 heterojunctions[14], the scattering times and plasmon frequencies of holes in the CdSe/GeO_2 film are much smaller. Remembering that Equation 1 is in good correlation with the classical mechanics solutions of differential equations subjected to electronic friction which exhibits damping coefficient of the form $\tilde{\beta} = 1/\tau_{n,p}$ and driven by sinusoidal alternating signals[15], then it is possible to conclude that the holes layer exhibit much higher damping coefficient compared to electrons layers.

Figure 6b show the conductivity (σ) spectra recorded in the frequency domain of 10-1800 MHz at ac signal amplitude of 0.10 V. The conductivity increases with increasing signal frequency up to 760 MHz. In the frequency domain of 760-1330 MHz, the conductivity decreases with increasing frequency. In the remaining range of frequency, the conductivity exhibits a local peak centered at 1635 MHz. Analysis of the conductivity spectra in accordance with the previously reported models of ac conduction reveals that the conductivity is dominated by the quantum mechanical tunneling (σ_{QMT}) in the low frequency domain and by the correlated barrier hopping (σ_{CBH}) in the high frequency domain. The total conductivity defined by the relation[14,16],

$$\sigma_{Tot.} = \left(\sigma_{QMT}^{-1} + \sigma_{CBH}^{-1}\right)^{-1} \quad (2)$$

with

$$\sigma_{QMT}(w) = \frac{\pi^4}{24} e^2 kT \alpha^{-1} (N(E_F))^2 w \left(\ln\left(1/(w\tau_0)\right)/(2\alpha)\right)^4 \quad (3)$$

and

$$\sigma_{CBH}(w) = \sigma_H(w) + \left(\sigma_L(w) - \sigma_H(w)\right) / \left(1 + w^2 \tau_{hop}^2\right). \quad (4)$$

In the above equations, $N(E_F)$ is the density of localized states near the Fermi level and τ_{hop} is the scattering time of hopping charged particles. α is spatial decay parameters for wave functions employed to describe the localized state at each site. α is accepted to be constant for all sites ($\alpha^{-1} = 10$ °A). τ_o is the inverse of the dominant phonon frequency ($\nu = 1/\tau_o$) in the studied interfaces. The subscript symbols H and L indicates the high and low frequency saturation conductivities, respectively. The fitting of the σ_{QMT}, σ_{CBH} and $\sigma_{Tot.}$ are shown in Figure 6b. The related fitting parameters which revealed good correlation between the theoretically estimated and experimentally measured conductivities are shown in Table 1. In accordance with the table, the scattering time needed for hoping of charged

Table 1. The ac conduction parameters for Au/CdSe/GeO_2/C MOSFET devices.

parameter	Value
τ_{hop} (ns)	9.91
ν (cm^{-1})	333.33
$N(E_F)$ ($x10^{18}$ $cm^{-3}eV$)	9.60
$\sigma(L)$ x (10^{-2} $\Omega^{-1}cm^{-1}$)	3.50
$\sigma(H)$ x (10^{-6} $\Omega^{-1}cm^{-1}$)	1.00
C_o (pF)	10.00
a_n	0.05
a_p	-0.55
τ_n (ns)	18.0
τ_p (ns)	0.42
W_n (MHz))	10.00
W_p (MHz)	10.00

particles through correlated barriers is the same as that we found for scattered holes and scattered electrons (estimated from capacitance spectra modeling). The estimated phonon frequency value being ~333 cm^{-1} is consistent with that reported as 333 cm^{-1} for transverse optical phonons in the E_u mode of oscillation of GeO_2[10]. The good consistency between the experimentally determined and theoretically estimated conductivity and capacitance spectral data assures the domination of the quantum mechanical tunneling at low frequencies below 760 MHz and the domination of correlated barrier hopping at high frequencies[15-18]. The poor fitting of the total conductivity at high frequencies (1000-1600 MHz) can ascribed to the existence of more than one kind of correlated and tunneling barriers which needs additional fitting to explore its origin[19].

It is interesting to mention the existence of the wide band gap GeO2 layer has remarkable roles on achieving band filter characteristics. Earlier studies on Au/CdSe indicated that optimizing a microwave band filter characteristics is not possible unless the CdSe layers are sandwiched with Yb nanosheets of thicknesses of 40 nm[6]. For Au/CdSe/Yb/CdSe/C devices, band stop filter characteristics with notch frequency of ~1500 MHz[6]. Yb/CdSe/C[20] tunneling barriers also did not display microwave band filter characteristics. For CdSe substrates achieving band filter characteristics always need to be stacked with materials having wider energy band gaps. As for examples, coating CdSe (E_g=1.78 eV) onto CdS (E_g = 2.42 eV) or onto GaSe (E_g = 2.10eV)[21,22] enabled CdSe exhibiting microwave resonator characteristics. In addition to this feature, in most of the mentioned heterojunctions that are comprising CdSe[6,19-22], inverted two MOSFET characteristics is not observed. As a result coating CdSe with GeO_2 is necessary for allowing multifunctionalities of the CdSe/GeO_2 interfaces.

4. Conclusions

In the current study, we have shown that it is possible to fabricate a metal- oxide-semiconductor field's effect transistor (MOSFET) from the CdSe/GeO_2 heterojunctions coated onto Au substrate and top contacted with carbon point contacts. The fabricated MOSFET devices are found to be beneficial for use as passive mode devices. The formed energy bands diagrams which is verified by the capacitance-voltage characteristics indicated the workability for both of the PMOS and NMOS channels appropriately. The capacitance and conductance spectra which are studied in the frequency domain that extends to microwave regions assure the usability of this device as microwave cavities.

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